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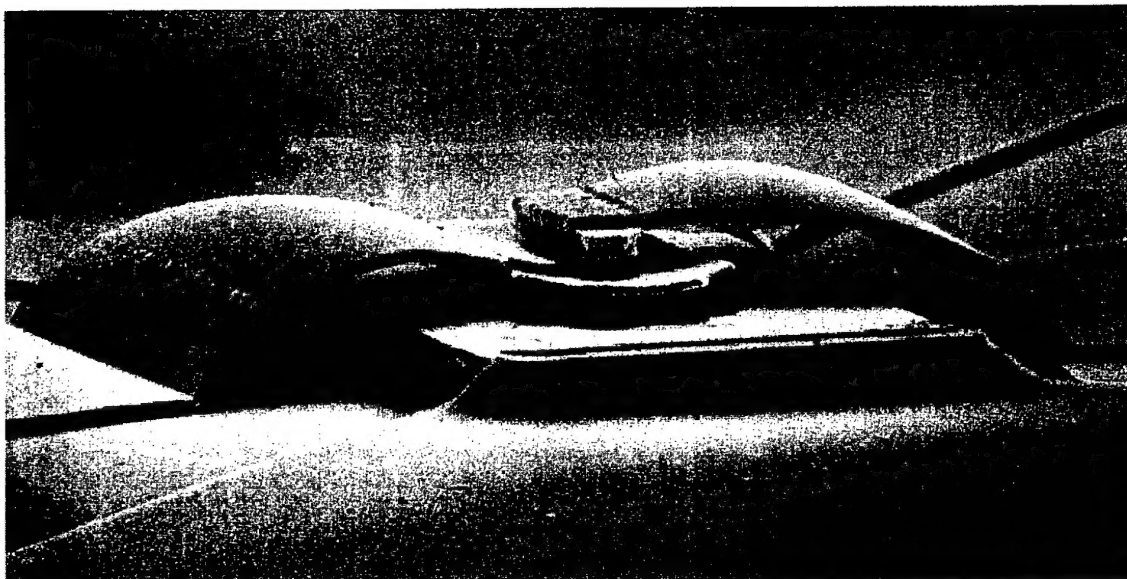


France Telecom

# WOCSDICE'99

23<sup>rd</sup> Workshop on Compound Semiconductor Devices  
and Integrated Circuits

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May 26-28, 1999

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# Summary

|  |     |
|--|-----|
| Advisory and organizing committees ..... | 4   |
| Schedule of events .....                 | 5   |
| Plenary session .....                    | 13  |
| Optoelectronic 1 .....                   | 25  |
| Reliability and Noise .....              | 37  |
| Technology .....                         | 57  |
| MMIC .....                               | 69  |
| Optoelectronic 2 .....                   | 85  |
| HBTs .....                               | 99  |
| Nitrides .....                           | 115 |
| New devices .....                        | 135 |
| Author index .....                       | 151 |

# Committees

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# Schedule of events

## Tuesday May, 25

17h00 – 19h00 : Registration and Get together party

19h30 – : Dinner

## Wednesday May, 26

08h50 – 09h00 : Opening session

09h00 – 10h45 : Plenary session

- *The market of the III–V semiconductors (invited paper)* p. 15  
Linh T. Nuyen  
Picogiga, Courtaboeuf, France
- *SiGe transistors and applications (invited paper)* p. 17  
Hermann Schumacher, U. Erben, W. Dür, K–B Schad, E. Sönmez, and P. Ebele  
University of Ulm, Ulm, Germany
- *InP–based HEMT ICs and their application toward Tbits/s transmission systems (invited paper)* p. 21  
Yasunobu Ishii  
NTT Photonics Laboratories, Kanagawa, Japan

10h45 – 11h15 : Coffee break

11h15 – 11h30 : Optoelectronic 1

- *Exploring new frontiers in semiconductor lasers: violet/blue GaN lasers and mid–infrared quantum cascade lasers (invited paper)* p. 27  
Daniel Hofstetter, J. Faist, M. Beck, U. Oesterle<sup>(1)</sup>, and D.P. Bour<sup>(2)</sup>  
University of Neuchâtel, Neuchâtel, Switzerland  
<sup>(1)</sup> EPFL, Lausanne, Switzerland  
<sup>(2)</sup> Xerox, Palo Alto CA USA
- *Tunnel–Junction–Connected Cascade Laser* p. 31  
A.N. Korshak, Z.S. Gribnikov, and V.V. Mitin  
Wayne State University, Detroit, MI USA

- *Low Avalanche Multiplication Noise in GaAs, GaAlAs and InP Sub-Micron PIN Diodes* p. 33  
J.P.R. David, K.F. Li, D.S. Ong, G.J. Rees, P.N. Robson, and R.C. Tozer  
University of Sheffield, Sheffield, UK
- *High Efficient  $Al_{0.1}Ga_{0.9}As$  Solar Cells* p. 35  
L. Semra, M. Remram, and A. Laugier<sup>(1)</sup>  
University of Constantine, Constantine, Algeria  
<sup>(1)</sup> LPM-INSA, Lyon, France

### 12h30 – 14h00 : Lunch

### 14h00 – 15h42 : Reliability and Noise

- *Hot electrons and reliability in HEMTs (invited paper)* p. 39  
Enrico Zanoni, G. Meneghesso, D. Buttari, M. Maretto, and G. Massari  
University of Padova, Padova, Italy
- *Comparison of the electrostatic discharge sensitivity of 1300nm lasers and light emitting diodes* p. 43  
H.C. Neitzert and A. Piccirillo  
Centro Studi e Laboratori Telecomunicazioni (CESLT), Torino, Italy
- *Reliability evaluation of GaAs HBT Technologies* p. 45  
C. Maneux, N. Labat, N. Saysset, A. Touboul, Y. Danto, JM. Dumas<sup>(1)</sup>, M. Riet<sup>(2)</sup>, and A. Scavennec<sup>(2)</sup>  
University of Bordeaux-IXL, Talence, France  
<sup>(1)</sup> University of Limoges-ENSIL, Limoges, France  
<sup>(2)</sup> OPTO+/CNET, Marcoussis, France
- *Three-terminal off-state breakdown in AlGaAs/GaAs power HFETs : a temperature-dependent analysis of the gate reverse current* p. 47  
D. Dieci, P. Cova<sup>(1)</sup>, R. Menozzi<sup>(1)</sup>, C. Lanzieri<sup>(2)</sup>, G. Meneghesso<sup>(3)</sup>, and C. Canali.  
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<sup>(2)</sup> Alenia systems, Roma, Italy  
<sup>(3)</sup> University of Padova, Padova, Italy
- *Electroluminescence of composite channel AlInAs / InGaAs / InP / AlInAs HEMTs* p. 49  
N. Cavassilas, F. Aniel, P. Boucaud, R. Adde, H. Maher<sup>(1)</sup>, J. Décobert<sup>(1)</sup>, and A. Scavennec<sup>(1)</sup>  
University of Orsay-IEF, Orsay, France  
<sup>(1)</sup> OPTO+/CNET, Marcoussis, France
- *Influence of deep levels in InAlAs/GaInAs/InP HFETs* p. 51  
A. Souifi, B. Georgescu, G. Brémond, M. Py<sup>(1)</sup>, J. Décobert<sup>(2)</sup>, G. Post<sup>(2)</sup>, and G. Guillot  
LPM-INSA, Lyon, France  
<sup>(1)</sup> EPFL, Lausanne, Switzerland  
<sup>(2)</sup> OPTO+/CNET, Marcoussis, France
- *Low frequency noise comparison between InP/InGaAs and Si/SiGe heterojunction bipolar transistors* p. 53  
S.G. Jarrix, C. Delseny, A. Penarier, F. Pascal, S. Blayac<sup>(1)</sup>, and P. Llinares<sup>(2)</sup>  
University of Montpellier-CEM2, Montpellier, France  
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<sup>(2)</sup> ST Microelectronics, Crolles, France

- *Interwell-transfer noise in InP-based InGaAs channels caused by electron tunneling at equilibrium and low electric fields* p. 55  
A. Matulionis, V. Aninkevicius, and J. Liberis  
Semiconductor Physics Institute, Vilnius, Lithuania

#### 15h55 – 16h25 : Coffee break

#### 16h25 – 17h39 : Technology

- *Doping profile extraction method with the sub-Debye length resolution* p. 59  
M.F. Kokorev, N.A. Maleev<sup>(1)</sup>, and A.G. Kuzmenkov  
State Electrotechnical University, Saint-Petersburg, Russia  
<sup>(1)</sup> A.F. Ioffe Physico-Technical Institute, Saint-Petersburg, Russia
- *Very high selective wet etching : application to the uniformity improvement of linear power PHEMT* p. 61  
X. Hue, B. Boudart, B. Bonte, and Y. Crosnier  
University of Lille-IEMN, Villeneuve d'Ascq, France
- *Small-size ohmic contacts to AlGaAs semiconductor devices* p. 63  
T.A. Briantseva, D.V. Lioubchenko, and V.E. Lyubchenko  
Institute of Radioengineering and Electronics, Moscow, Russia
- *Indium tin oxide spreading layers for high performance visible LED's* p. 65  
D.V. Morgan, I.M. Al-Ofi, and Y.H. Aliyu  
Cardiff University, Cardiff, UK
- *The present state of production and development of III-V compounds in Elma-Malachit* p. 67  
A. Arendarenko and Yu Sveshinikov  
JSC Elma-Malachit, Moscow, Russia

#### 17h40 – 19h10 : MMIC

- *GaAs MHEMT: The evolution of GaAs-based FETs for high performance microwave and millimeter wave low noise applications (invited paper)* p. 71  
Thomas Kazior  
Raytheon Microelectronics, Andover, MA USA
- *A 94 GHz CPW low noise amplifier on InP* p. 75  
V. Hoel, S. Boret, B. Grimbert, G. Apercé<sup>(1)</sup>, T. Decaesteke<sup>(1)</sup>, S. Bollaert, X. Wallart, S. Lepilliet, and A. Cappy  
University of Lille-IEMN, Villeneuve d'Ascq, France  
<sup>(1)</sup> Thomson-Detexis, St Cloud, France
- *High-efficiency MMIC power amplifiers using AlGaAs p-HEMT technology* p. 77  
D. Roques, J-C. Sarkissian, B. Cogo, M. Soulard, J-L. Cazaux, J. Malin<sup>(1)</sup>, D. Shaw<sup>(1)</sup>, and D. Simpson<sup>(1)</sup>  
Alcatel Space Industries, Toulouse, France  
<sup>(1)</sup> Tri-Quint Semiconductor Texas, USA
- *GaAs PHEMT spice model for very high bit rate digital circuits.* p. 79  
D. Demange and R. Leblanc  
Philips Microwave Limeil, Limeil Brevannes, France

- *Composite channel InP HEMT for high cut-off frequency x breakdown voltage performance* p. 81  
C. Ladner, J. Décobert, S. Sainson, S. Biblémont, G. Post, M. François<sup>(1)</sup>, M. Müller<sup>(1)</sup>  
OPTO+/CNET, Marcoussis, France  
<sup>(1)</sup> University of Lille-IEMN, Villeneuve d'Ascq, France
- *Characterization of residual carbon in semi-insulating GaAs substrates for integrated circuits* p. 83  
K.D. Glinchuk, N.M. Litovchenko, A.V. Prokhorovitch, and O.N. Strilchuk  
Institute of Semiconductors Physics, Kyiv, Ukraine

19h30 – : Dinner

## Thursday May, 27

### 09h00 – 10h20 : Optoelectronic 2

- *PBG in two-dimensions : from concepts to applications (invited paper)* p. 87  
Henri Benisty, D. Labilloy, C. Weisbuch, T.F. Krauss<sup>(1)</sup>, C.J.M. Smith<sup>(1)</sup>, R.M. De La Rue<sup>(1)</sup>,  
R. Houdré<sup>(2)</sup>, and U. Oesterle<sup>(2)</sup>  
Ecole Polytechnique-LPMC, Palaiseau, France  
<sup>(1)</sup> University of Glasgow, Glasgow, UK  
<sup>(2)</sup> EPFL, Lausanne, Switzerland
- *High Q-factor 2D photonic bandgap microcavities on InP-based suspended membranes* p. 91  
P. Pottier, C. Seassal, X. Letartre, J.L. Leclercq, P. Viktorovitch, D. Cassagne<sup>(1)</sup>, and C. Jouanin<sup>(1)</sup>  
Ecole Centrale de Lyon-LEOM, Lyon, France  
<sup>(1)</sup> University of Montpellier-GES, Montpellier, France
- *Responsivity enhancement in GaInAs/InAlAs/InP OPFETs by backgating* p. 93  
U. Hodel, M. Marso, A. Fox, A. Förster, and P. Kordos  
Institute of Thin Film and Ion Technology, Jülich, Germany
- *Design and first results on a vertical integrated transistor-laser structure for high-speed low-chirp modulation* p. 95  
R.C.P. Hoskens, B. Ljevar, G. Archontopoulos, V.I. Tolstikhin, and T.G. van der Roer  
Technische Universiteit Eindhoven, Eindhoven, Netherlands
- *Investigation of a PIN laser cleaved surface using Kelvin probe force microscopy and 2D physical simulations* p. 97  
F. Robin, H. Jacobs, O. Homan, A. Stemmer, and W. Bächtold  
ETH Center, Zurich, Switzerland

### 10h20 – 10h50 : Coffee break

### 10h50 – 12h15 : HBTs

- *High efficient AlGaAs/GaAs HBTs for Mobile Communications* p. 101  
M. Achouche, S. Kraus, S. Hahle, W. John, M. Mai, D. Rentner, T. Spitzbart, P. Wolter,  
H. Wittrich, T. Bergunde, F. Brunner, P. Kurpas, E. Richter, M. Weyers, J. Würfl, G. Tränke  
FBH, Berlin, Germany

- *RF power HBTs: modelling and optimization of the electrothermal behavior* p. 103  
P. Souverain, T. Camps, J. Tasselli, A. Cazarré, A. Marty, and J.P. Bailbé  
LAAS-CNRS, Toulouse, France
- *Evidence and characterization of ballistic transport in InP-based HBTs* p. 105  
D. Sicault, R. Teissier, J-L. Pelouard, F. Pardo, and F. Mollot  
L2M-CNRS, Bagneux, France
- *High performance InP based technology for optoelectronic applications* p. 107  
C. Bergamaschi, A. Huber, D. Huber, V. Schwarz, M. Rohner, T. Morf, and H. Jäckel  
ETH Center, Zürich, Switzerland
- *Self-aligned InP/InGaAs double heterojunction bipolar transistors for high bit-rate circuit applications* p. 109  
M. Riet, S. Blayac, J-L. Benchimol, P. André, P. Berdager, A-M. Duchenois, J. Godin.  
OPTO+/CNET, Marcoussis, France
- *Size effects in low InP/InGaAs DHBTs* p. 111  
S. Blayac, M. Riet, J-L. Benchimol, A-M. Duchenois, P. Berdager, J-P. Medus, and J. Godin  
OPTO+/CNET, Marcoussis, France
- *High speed collector-up MHBTs* p. 113  
S. Demichel, F. Pardo, R. Teissier, and J-L. Pelouard  
L2M-CNRS, Bagneux, France

## 12h30 – 14h00 : Lunch

## Friday May, 28

## 09h00 – 10h55 : Nitrides

- *Group III-Nitride semiconductor transistors for power amplifiers (invited paper)* p. 117  
John C. Zolper  
Office of Naval Research, Arlington, VA USA
- *MOCVD grown AlN/GaN HFETs* p. 121  
E. Alekseev, A. Eisenbach, and D. Pavlidis  
University of Michigan, Ann Arbor, MI USA
- *Single and double barrier AlGaIn/GaN modulation doped field effect transistors grown by RF assisted MBE* p. 123  
A. Vescan, A. Wieszt, R. Dietrich, H. Leier, N. Käß<sup>(1)</sup>, E. Kohn<sup>(1)</sup>, J.M. Van Hove<sup>(2)</sup>, P.P. Chow<sup>(2)</sup>, and A.M. Wowchak<sup>(2)</sup>  
DaimlerChrysler AG, Ulm, Germany  
<sup>(1)</sup> University of Ulm, Ulm, Germany  
<sup>(2)</sup> SVT Associates, Eden Prairie, MN USA
- *GaN Static Induction Transistor Fabrication* p. 125  
N.G. Weimann and L.F. Eastman  
Cornell University, Ithaca, NY USA
- *GaN MESFETs for high temperature applications* p. 127  
S. Trassaert, B. Boudart, C. Gaquière, D. Théron, Y. Crosnier, F. Huet<sup>(1)</sup>, M.A. Poisson<sup>(1)</sup>  
University of Lille-IEMN, Villeneuve d'Ascq, France  
<sup>(1)</sup> Thomson CSF-LCR, Orsay, France

- *Power performance of AlGaIn/GaN HEMTs with 0.2 to 1 mm gate widths* p. 129  
E. Alekseev, D. Pavlidis, N.X. Nguyen<sup>(1)</sup>, C. Nguyen<sup>(1)</sup>, and D.E. Grider<sup>(1)</sup>  
University of Michigan, Ann Arbor, MN USA  
<sup>(1)</sup> HRL Laboratories, Malibu, CA USA
- *How to explain the high breakdown voltages (>200V) in GaN-based HFET with high channel sheet charge (>10<sup>13</sup> cm<sup>-2</sup>)?* p. 131  
I. Daumiller, P. Schmid, E. Strobel, and E. Kohn  
University of Ulm, Ulm, Germany
- *Biologically weighted UV-meters based on AlGaIn schottky barrier photodetector* p. 133  
E. Monroy, F. Calle, E. Muñoz, F. Omnès, and P. Gibart  
ETSI Telecomunicación, Madrid, Spain  
CRHEA-CNRS, Valbonne, France

#### 10h55 – 11h25 : Coffee break

#### 11h25 – 12h54 : New devices

- *Highly non linear devices for operation at Terahertz frequencies (invited paper)* p. 137  
Didier Lippens  
University of Lille-IEMN, Villeneuve d'Acsq, France
- *Resonant Tunneling Diodes for High-Speed Trigger Applications* p. 141  
F. Yousif, M. Kunze, K. Bitzer, and H. Schumacher  
University of Ulm, Ulm, Germany
- *A 150 GHz MMIC Receiver Array with On-Chip Pumping-Power Distribution for Plasma ECE Disgnostics* p. 143  
M. Rodríguez-Gironés, J.P. Pascual<sup>(1)</sup>, M.L. de la Fuente<sup>(1)</sup>, F. Lopez, C.I. Lin, A. Simon, and H.L. Hartnagel  
Technical University of Darmstadt, Darmstadt, Germany  
<sup>(1)</sup> University of Cantabria, Santander, Spain
- *Hot Electron Injection Field Effect Transistor* p. 145  
E. Kolmhofer, M. Bergmair, C. Diskus, K. Luebke, A. Stelzer, and H. Thim  
University of Linz, Linz, Austria
- *Modulation Response Predictions for a Dual Channel SiGe FET* p. 147  
G.C. Crow and R.A. Abram  
University of Durham, Durham, United Kingdom
- *Piezoelectric and Optical Properties of Strained InGaAs/GaAs Quantum Well Structures Grown by MOVPE on (111)A GaAs Substrates* p. 149  
S. Cho, J. Kim, A. Sanz-Hervás, A. Majerfeld, P. Tronc<sup>(1)</sup>, C. Villar<sup>(2)</sup>, B.W. Kim<sup>(3)</sup>  
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#### 12h55 – 13h00 : Closing session

#### 13h15 – 14h45 : Lunch

# Notes

**Wednesday, May 26, 1999 9:00 am**

## Plenary session

- *The market of the III-V semiconductors (invited paper)* p. 15  
Linh T. Nuyen  
Picogiga, Courtaboeuf, France
- *SiGe transistors and applications (invited paper)* p. 17  
Hermann Schumacher, U. Erben, W. Dürr, K-B Schad, E. Sönmez, and P. Ebele  
University of Ulm, Ulm, Germany
- *InP-based HEMT ICs and their application toward Tbits/s transmission systems (invited paper)* p. 21  
Yasunobu Ishii  
NTT Photonics Laboratories, Kanagawa, Japan

## **The Market of the III–V semiconductors.**

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# SiGe Transistors and Applications

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## 1 Introduction

The increasing use of wireless techniques in the distribution of multimedia content to fixed and mobile users necessitates an expansion of the frequency range useable for consumer services. Keeping cost down is a major challenge. Silicon-based MMICs become increasingly interesting because they promise to exploit the vast technology base developed for large-scale integrated circuits. Silicon bipolar transistors have long been the mainstay of Si MMICs below 3 GHz, where CMOS becomes increasingly attractive. Frequencies beyond 3 GHz, however, are traditionally being served by III-V semiconductor devices. We have explored the performance potential of a commercially available SiGe heterojunction bipolar technology in this frequency range, concentrating on integrated circuits for receiver front-ends.

## 2 SiGe heterostructure bipolar transistors

From the beginning, the development of SiGe HBTs has been carried out along two quite different lines of thought. One approach, championed by IBM and followed by a number of other companies, uses a triangular Ge profile in the base, starting with a mole fraction of zero at the base emitter junction and increasing to a value of typically 15 % at the base collector junction. The resulting change in band gap creates a strong electric field in the base and hence reduces the base transit time. The ratio of emitter and base doping concentrations in these transistors is similar to Si homojunction bipolar transistors. A low base resistance can be achieved by aggressive lateral scaling of the emitter.

The other approach, mostly developed at the Daimler Chrysler Research Center [1] and, more recently, at Temic Semiconductors GmbH [2], uses a constant Germanium profile in the base, with a Ge concentration in excess of 20 %. Here, the resulting emitter-base heterojunction provides an efficient barrier against the unwanted injection of base majority carriers into the emitter. The base doping concentration can be increased and the emitter doping concentration decreased. The base sheet resistance and the emitter-base junction capacitance can be lowered. In these transistors, there is no need for deep-sub- $\mu\text{m}$  emitter widths. Much-improved maximum frequencies of oscillation, with a record value of 160 GHz [3], have been demonstrated with an emitter width of 0.8  $\mu\text{m}$ .

The integrated circuits discussed in this paper have been fabricated at Temic Semiconductor GmbH. The transistors have a planar geometry where the SiGe base and epitaxial emitter are formed by differential epitaxy. The Ge mole fraction in the 30 nm wide base is 20 %, with a boron concentration of  $4.5 \times 10^{19} \text{ cm}^{-3}$ . With 1.2  $\mu\text{m}$  emitter width,  $f_T=35$  GHz and  $f_{\text{max}}=50$  GHz have been demonstrated. Using a different collector doping profile available on the same wafer through selective collector implants, the transit frequency can be increased to 50 GHz while maintaining  $f_{\text{max}}$ , though lowering the breakdown voltage. The substrate for these "box-shaped" planar HBTs has a specific resistivity of 20  $\Omega\text{cm}$ . MIM capacitors with a specific capacitance of 1.1 fF/ $\text{cm}^{-2}$  are available, and spiral inductors have been demonstrated with Q values upto 10.

### 3 Circuit examples

The 5-6 GHz frequency range is attracting much attention lately for wireless local area network (WLAN) applications like the European HiperLAN, avoiding the spectral congestion at lower frequencies. The LNA to be discussed in more detail here uses the production-type SiGe technology as outlined above. A common-emitter design has been adopted here with a parallel-resonant reactive load circuit. The input transistor size has been chosen to  $2 \times 1.2 \times 20 \mu\text{m}^2$  to properly locate the noise-optimum source reflection coefficient  $\Gamma_{\text{opt}}$ , further aided by the inductive emitter feedback in the first transistor. A common-collector second stage provides the output match and ensures a high first-stage load impedance.

For the measurement, the amplifier was biased at 4.5 V and 7.4 mA. As **Fig. 1** shows, a minimum noise figure of 1.5 dB and an associated gain of 23 dB were achieved. The IC minimum noise figure corresponds closely to the value measured for individual transistors on the same wafer.

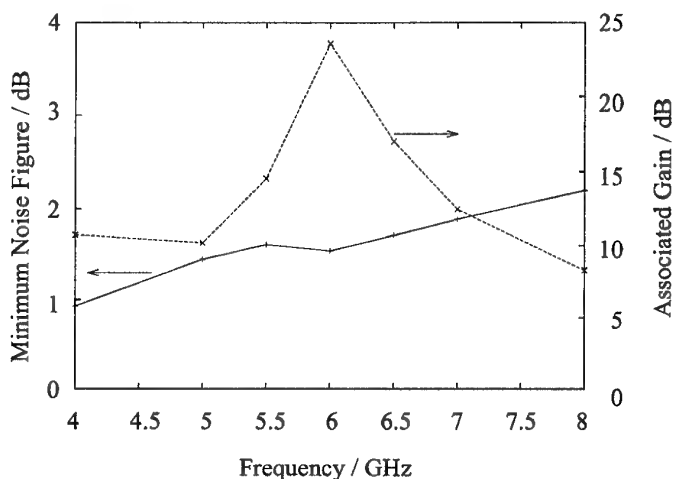


Figure 1: Measured minimum noise figure and associated gain at input noise match for the 5.8 GHz SiGe LNA [4]

The 10 GHz amplifier uses a Cascode gain stage with a reactive load in parallel resonance at the frequency of operation. The gain stage transistors have a size of  $2 \times 1.2 \times 20 \mu\text{m}^2$ , a compromise between location of the noise optimum source impedance and the devices' minimum noise figure, which increases at smaller sizes. Output decoupling is provided by a common-collector stage. **Fig. 2** shows the circuit schematic.

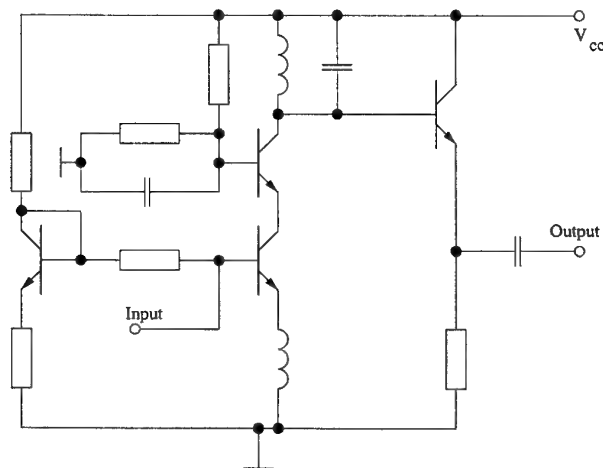


Figure 2: Circuit diagram of the 10 GHz SiGe HBT LNA [5]

Due to the Cascode gain stage and the resonant load, the associated gain is sufficiently high at 15 dB. The minimum noise figure at the design frequency of 10.5 GHz was 3.3 dB. A possible use of the LNA will be in a two-chip downconverter system formed by a III-V pseudomorphic HEMT connected to a SiGe chip including further low-noise amplification, mixing, VCO, IF amplification, and bias circuitry.

Aside from low-noise amplifiers, we also investigated active mixers in the 5-12 GHz frequency range. **Fig. 3** shows the circuit schematic of a 11 GHz mixer with a 1250 MHz IF. The local oscillator and RF signals are injected in single-ended configuration into a Gilbert cell mixing stage. The transistor sizes and bias points were optimized for minimum noise figure and ease of noise matching at the RF port. The output of the Gilbert cell is reactively matched to the input of the subsequent IF amplifier (T9 through T12) to obtain a flat conversion gain over the wide IF band of 500 MHz. T14 through T16 provide differential to single-ended conversion.

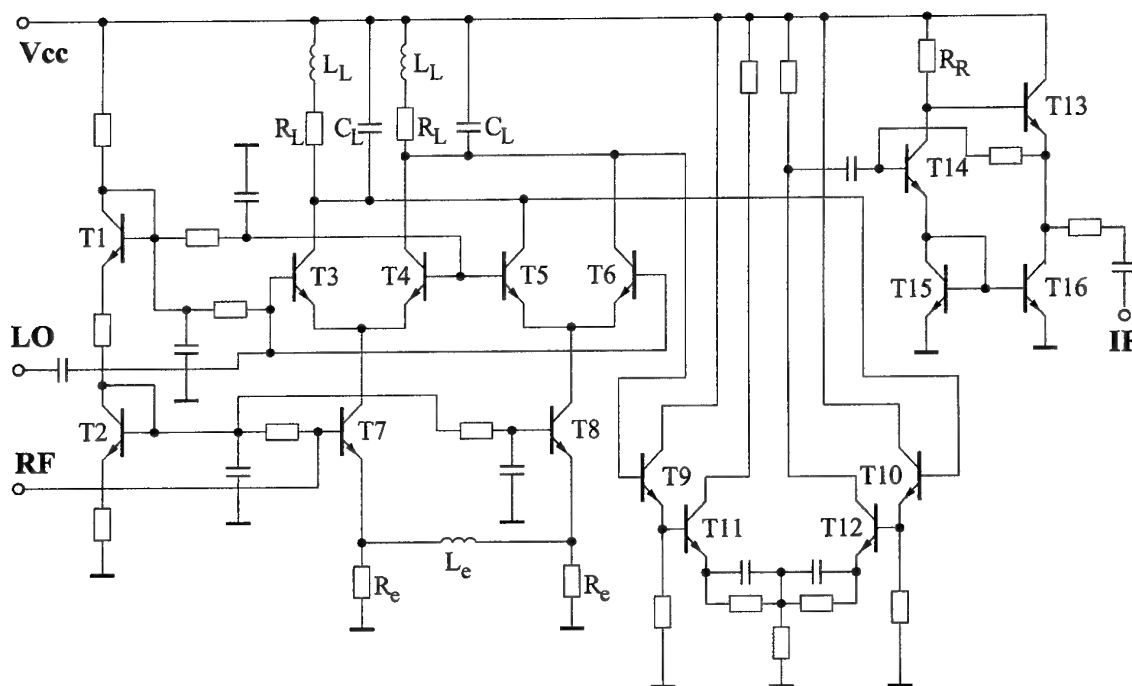


Figure 3: Circuit schematic of an 11 GHz SiGe HBT receive mixer [6]

Drawing only 53 mW from a 3.6 V supply, the mixer provides 16.1 dB conversion gain and a double-sideband noise figure of 9.4 dB at 1250 MHz IF. The local oscillator power, at 9.75 GHz, was -2 dBm. This is to our knowledge the lowest noise figure for a Si-based active mixer at that frequency. The simulated and measured data agrees very well, confirming the validity of our MEXTRAM nonlinear SiGe HBT models even at this high frequency.

## 4 Conclusion

We presented components for consumer microwave systems using a production SiGe HBT process with high Ge mole fraction in the base. The low base sheet resistance enables transistors with cutoff frequencies of 50 GHz and superior microwave noise performance despite relaxed lateral scaling rules of 1.2  $\mu\text{m}$ .

The performance potential has been evaluated in low-noise amplifiers and active mixers for 5.8 GHz and 11 GHz. The LNAs exhibited minimum noise figures of 1.5 dB at 5.8 GHz and 3.3 dB at 11 GHz, while the Gilbert cell mixer at 11 GHz had a minimum noise figure of 9.4 dB and a 16 dB conversion gain.

Following our experiments, we believe that SiGe MMICs are an attractive, readily available option for MMICs targeting consumer markets in the 2-12 GHz range. Because prototype transistors have shown that

SiGe HBTs can reach cutoff frequencies in excess of 100 GHz, it can be predicted that SiGe MMICs will also be able to meet the opportunities arising in the 20-30 GHz range in the near future.

## 5 Acknowledgements

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# InP-based HEMT ICs and Their Application Toward Tbit/s Transmission Systems

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## Introduction

The upcoming explosive demand for multimedia services will require ultrahigh capacity networks above the Tbit/s level. High-speed digital IC technology is the key for electrical time-division multiplexing (ETDM), which determines the basic channel data rates of each channel. The subsequent passive optical multiplexing, such as wavelength multiplexing (WDM) and optical time-division multiplexing (OTDM), gathers each channel with up to Tbit/s level capacity into a single fiber. InP-based HEMTs consisting of an InAlAs/InGaAs heterostructure have achieved record current gain cutoff frequency and are considered to be promising candidates for high-speed ICs. This paper describes state-of-the-art InP-based HEMT digital IC technologies and applications to 40-Gbit/s ETDM as the core of future Tbit/s transmission systems.

## Basic Device Technologies

The basic device structure features MOCVD-grown heterostructure comprising an InP recess-etch stopper, an  $n^+$ -InAlAs/ $n^+$ -InGaAs cap layer, a separated level shift diode, and a novel T-shaped gate (Fig. 1).

**Heterostructure:** The heterostructure is grown by MOCVD at 630°C on a semi-insulating InP substrate. The epitaxial structure consists of a 200-nm-thick InAlAs buffer, a 15-nm-thick InGaAs channel, a 3-nm-thick InAlAs spacer, a Si- $\delta$ -doped plane, a 6-nm-thick InAlAs Schottky barrier, a 5-nm-thick InP-recess-etch stopper, and  $n^+$ -InAlAs/ $n^+$ -InGaAs cap layers. All layers are lattice-matched to InP. The thin InP recess-etch stopper grown at a high  $\text{PH}_3$  flow rate drastically improves recess-etch-stopping ability. This stopper layer not only assures the uniformity of threshold voltage but also enables exact design of the device, and allows us to integrate a dozen transistors for the particular circuit design. The highly doped  $n^+$ -InAlAs/ $n^+$ -InGaAs cap layer lowers the heterobarrier and increases the tunnel current at the InAlAs/InGaAs interface, and provides low-resistance contacts with non-alloyed metal for source and drain electrodes [1-4].

**0.1- $\mu\text{m}$ -gate structure:** For precise, uniform, and reproducible T-shaped 0.1- $\mu\text{m}$ -long gates, the bottom of the T-gate is patterned by electron beam (EB) lithography and then the top is patterned by photo lithography. This process makes it possible to use thin single-layer EB resist, which is beneficial for high resolution. We utilize a 25-keV EB direct writer with a durable EB resist, ZEP, to delineate the gate footprint. The footprint pattern is then replicated on the  $\text{SiO}_2/\text{SiN}$  films by reactive ion etching (RIE). During RIE, the aspect ratio of the opening is reduced by making a side etch in the top SiN layer for complete filling of the groove with the gate metal. After removing the EB resist, the gate recess region is selectively etched down to the InP recess-etch stopper through the opening in the  $\text{SiO}_2/\text{SiN}$  and the WSiN gate metal is deposited using a reactive sputter. The top part of the T-gate consists of Ti/Pt/Au and is deposited and lifted off [5] (Fig. 2).

**Nanocomposite resist for deep sub-0.1- $\mu\text{m}$ -gate:** For shorter gates below 0.1  $\mu\text{m}$  and down to 30 nm, we have used fullerene-incorporated nanocomposite EB resist for enhanced RIE resistance and pattern contrast.

A commercially available fullerene  $C_{60}$  was incorporated into ZEP to make a 10 wt%- $C_{60}$  solution ( $C_{60}$ -ZEP). The  $C_{60}$ -ZEP provides 10-20 % better RIE resistance than conventional ZEP. Thanks to RIE resistance, we can use thinner EB resist for higher resolution during the gate process. In addition, the fullerene molecules act as a strong dissolution inhibitor during development and therefore produce high-contrast patterns by minimizing film degradation at the corners of the pattern. Combining  $C_{60}$ -ZEP and the novel two-step-recess structure, we confirmed the highest  $f_T$  of 350 GHz with a 30-nm-gate [6-8] (Fig. 3).

**High-speed interconnection:** As device speed increases, the interconnection propagation delay begins to dominate circuit speed. Based on our previous air-bridged technology, the interconnection delay accounted for about 30 % of the total delay. To reduce interconnection delay, we have introduced two-level interconnection process using low-permittivity ( $\epsilon_r=2.8$ ) benzocyclobutene (BCB) as an inter-level dielectric. This interconnection technology not only allows dense layouts and reduced propagation delays but also enables us to make impedance-matched interconnections. We newly adopted a microstrip line (MSL) with a narrow second-layer conductor on top of the first layer. The MSL offers small line delay with increased propagation velocity and reduced signal distortion due to better impedance matching between SCFL output and interconnection. A record 80-Gbit/s MUX operation was attained using newly developed interconnections [9-12].

#### **IC chip set and packaging:**

High-speed multiplexer (MUX), demultiplexer (DEMUX), decision circuit (DEC), and frequency divider (DIV) ICs are key digital elements in transmitter and receiver hardware. A flip-flop (F/F) and a 2:1 selector (SEL) are core circuits for constructing these digital ICs. F/Fs are employed in DEC, DIV, MUX, and DEMUX, while SELs are used in MUX. We designed a digital IC chip set based on SCFL series gated circuitry. The maximum operating speed of D-F/Fs is lower than that of SELs when the same device technology is used because the clock frequency for SELs is half that for F/F at the same bit rate. Improving the F/F speed is the key to obtaining faster digital IC chip sets. A super-dynamic (SD) -D-F/F and a high-speed latching operation (HLO) -D-F/F are employed to enhance the operating speed of F/F-based ICs such as DEC, DIV, and DEMUX. Maximum operating speed of 80 Gbit/s for MUX and 46 Gbit/s for DIV have been confirmed in wafer measurement [13-15] (Fig. 4).

Packaging is another key technology for realizing ultra-broadband signal transmission without undesirable losses due to cavity and/or parasitic resonance and coupling. The basic structure we adopted is the so-called "chip-size cavity" package that minimizes the inner cavity. The RF ports are made with V-band coaxial connectors. The digital-type package can accommodate up to 6 RF ports. A die is mounted on an inner thin-film multilayer interconnection substrate by means of ribbon bonding. The internal metal lids reduce the size of the inner cavity so as to shift undesirable cavity resonance out of the transmission band. The module with metal lids had a high isolation of more than 60 dB up to 50 GHz. A microphotograph of the ribbon-bonded InP HFET MUX chip is shown in Fig. 5 [16].

#### **Prototyping and transmission experiment:**

A 40-Gbit/s optical transmitter and receiver system has been prototyped using an InP-based digital IC chip set. In the receiver unit, a UTC-PD module directly drives a D-F/F without an analog amplifier (Fig. 6). The receiver

showed a high-sensitivity of -21.8 dBm after 100-km-long dispersion-shifted fiber transmission. Four-channel 40-Gbit/s, 100-km long WDM transmission has been successfully performed. Ten-channel 40-Gbit/s (400 Gbit/s) WDM experiment based on the dispersion flattened fiber has also been carried out. [17-19]

**Summary:** This paper has reviewed the current status of InP-based HEMT ICs for lightwave communications in terms of device, circuit, packaging technologies, and system prototyping. All packaged ICs have achieved 40-Gbit/s operation by using 0.1- $\mu$ m gate InP HEMTs, high-speed designs, and broadband packaging technologies. 40-Gbit/s optical fiber transmission experiments were successfully carried out using an InP-ICs chip set. Our 40-Gbit/s data rate system is considered to be a promising technology for realizing practical Tbit/s communication systems.

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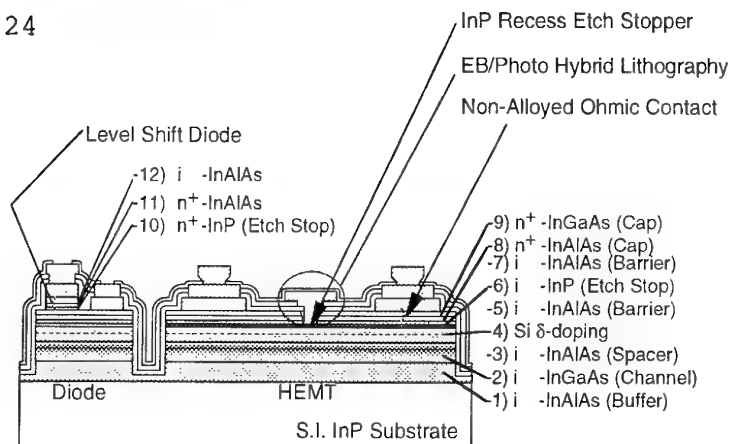


Fig. 1 Cross-sectional device structure

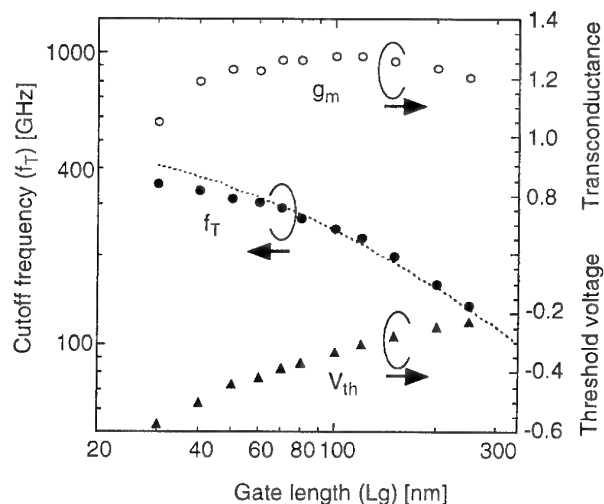
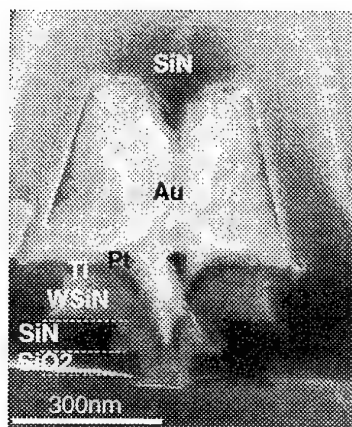
Fig. 3  $L_g$  dependence of device characteristic

Fig. 2 SEM cross-section of 0.1-μm T-gate

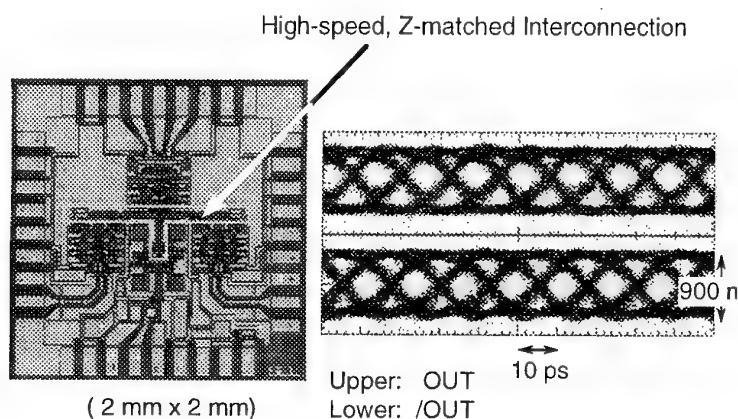


Fig. 4 Photomicrograph of MUX and operating waveform

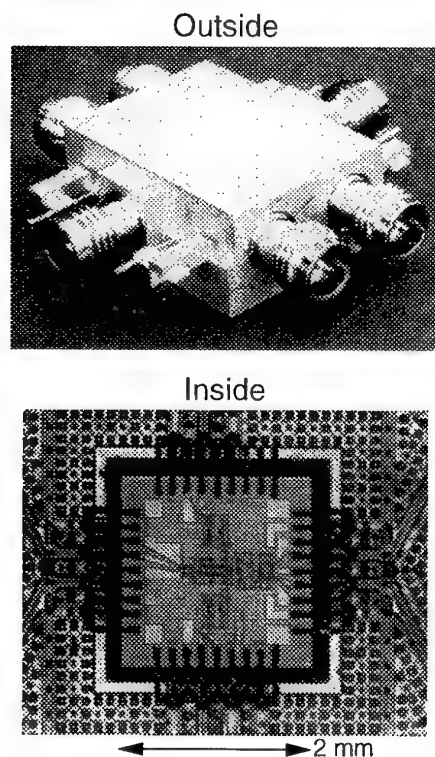


Fig. 5 Chip-size-cavity package with 6-RF ports

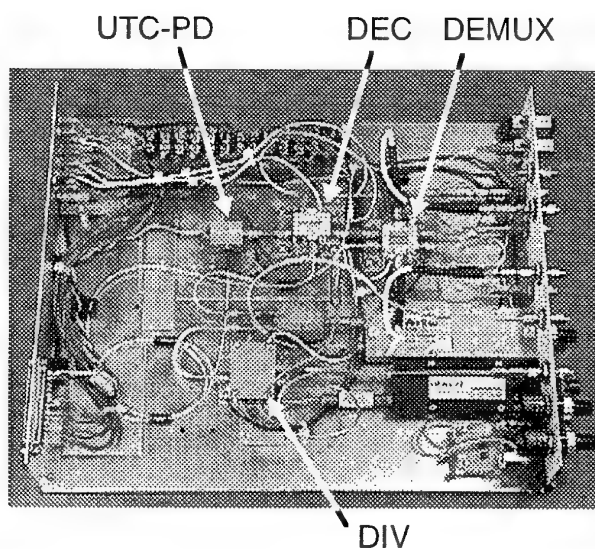


Fig. 6 40 Gbit/s receiver unit

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# Optoelectronic I

- *Exploring new frontiers in semiconductor lasers: violet/blue GaN lasers and mid-infrared quantum cascade lasers (invited paper)* p. 27  
 Daniel Hofstetter, J. Faist, M. Beck, U. Oesterle<sup>(1)</sup>, and D.P. Bour<sup>(2)</sup>  
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- *Tunnel-Junction-Connected Cascade Laser* p. 31  
 A.N. Korshak, Z.S. Gribnikov, and V.V. Mitin  
 Wayne State University, Detroit, MI USA
- *Low Avalanche Multiplication Noise in GaAs, GaAlAs and InP Sub-Micron PIN Diodes* p. 33  
 J.P.R. David, K.F. Li, D.S. Ong, G.J. Rees, P.N. Robson, and R.C. Tozer  
 University of Sheffield, Sheffield, UK
- *High Efficient Al<sub>0.1</sub>Ga<sub>0.9</sub>As Solar Cells* p. 35  
 L. Semra, M. Remram, and A. Laugier<sup>(1)</sup>  
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## Exploring new frontiers in semiconductor lasers: violet/blue GaN lasers and mid-infrared quantum cascade lasers

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The use of novel material systems and sophisticated epitaxial growth techniques recently led to the fabrication of both violet/blue and mid-infrared semiconductor lasers. For the short-wavelength devices, establishing growth capabilities for high-quality GaN/InGaAlN heterostructures was necessary. For the mid-infrared quantum cascade lasers, the use of intersubband transitions in the InGaAs/InAlAs material system instead of electron/hole recombinations in small bandgap materials led to a major breakthrough. While violet/blue semiconductor lasers will revolutionize optical data storage and laser printing businesses, the now available high-power mid-infrared lasers will have a great impact on gas sensing applications. Many important pollutants are absorbing in the so-called fingerprint region of the infrared spectrum. This is exactly in the wavelength range which is accessible by quantum cascade lasers. In this presentation, we would thus like to report the current status and some future trends in both of these research topics.

### Electrically injected InGaN/GaN DFB lasers at 400 nm

In the InGaN/GaN material system, we report the very recent demonstration of optically pumped and electrically injected distributed feedback lasers [1], [2]. The emission wavelength of these devices was centered at 400 nm. The fabrication of these devices relied on growing a 4  $\mu\text{m}$  thick n-type GaN:Si layer on C-face sapphire. On top of this layer, we grew a 500 nm thick, n-doped  $\text{Al}_{0.08}\text{Ga}_{0.92}\text{N}:\text{Si}$  lower cladding layer, a 100 nm thick n-doped GaN:Si lower waveguiding layer, a 30 nm thick un-doped active region with five 3 nm thick  $\text{In}_{0.15}\text{Ga}_{0.85}\text{N}$  quantum wells and 7 nm thick GaN barriers, and a 180 nm thick p-doped GaN:Mg upper waveguiding layer. For the electrically injected, index-coupled device, the 3<sup>rd</sup> order grating with a period of 240 nm was defined by a holographic exposure and dry-etched into the upper waveguiding layer by chemically-assisted ion beam etching. A numerical calculation

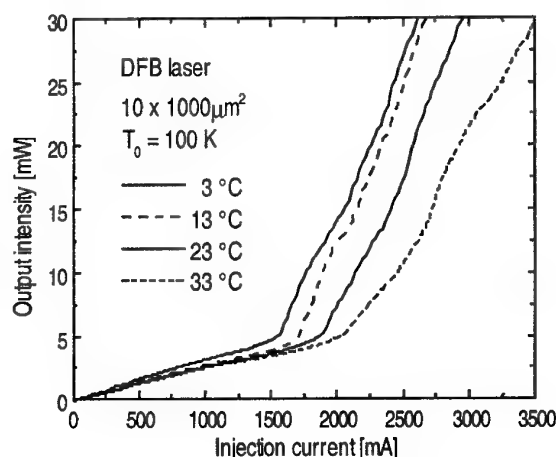


Fig. 1 - L-I-characteristics of an InGaN / GaN DFB laser with an active area of  $10 \times 1000 \mu\text{m}^2$  at four different heatsink temperatures.

of the coupling coefficient showed that the tooth shape of this 100 nm deep grating was a critical parameter. For our rectangular tooth geometry with rounded tops, the coupling coefficient was relatively weak, on the order of 5 - 10 cm<sup>-1</sup>. Together with a cavity length of 1000  $\mu$ m, this coupling strength corresponds to an effective reflectance of 15 - 30 %. After grating fabrication, we performed optical pumping experiments in order to confirm the matching between the grating resonance wavelength and the gain peak. Then, we proceeded with an epitaxial re-growth to complete the device structure. This re-growth consisted of a 300 nm thick p-doped Al<sub>0.08</sub>Ga<sub>0.92</sub>N:Mg upper cladding layer and a 100 nm thick p-type GaN:Mg contact layer.

Device processing for the electrically pumped devices involved the definition mesas to enable lateral n-type contacting of the devices, and evaporation of standard n- and p-metal Ti/Au layers. The p-metal contact stripes were 4, 10 or 20  $\mu$ m wide, and thus defined the width of the gain region. A SiON layer was used to electrically isolate the non-contacted areas and the sidewalls of the mesas, thereby restricting gain to within a narrow stripe in the lateral direction. Following the SiON window etch, we evaporated another Ti/Au layer in order to provide the p-metal contact pads for the probe. Finally, the mirrors were etched, again by chemically-assisted ion beam etching.

Measurements of the I-V- and L-I-characteristics were carried out under pulsed current conditions (500 ns pulse length, 0.05 % duty cycle) at room temperature. The lasers were probe contacted and tested on chip. As shown in the L-I-curves of figure 1, we obtained, for the longest devices with 10 microns stripe width, pulsed threshold currents of 1550 mA at 3 °C and 2050 mA at 33 °C. The best threshold currents were obtained on lasers with 20 microns stripe width and 1000  $\mu$ m cavity length. Values of 3200 mA for 20 microns wide devices were observed, corresponding to threshold current densities of 16 kA/cm<sup>2</sup>. For shorter devices with 20 microns stripe width, we measured higher threshold currents of 4600 mA (threshold current density of 23 kA/cm<sup>2</sup>). For the best devices, typical threshold voltages of  $V(I_{th}) = 16$  V were seen.

While there is only one clean peak with a resolution limited width of 0.5 Å for lower injection currents, there appear to be multiple peaks with an overall width of 5 Å at higher injection levels. The fact that all additional features occurred at the long wavelength side of the main peak suggests that chirping due to device heating during the current pulse is responsible for this kind of broadening. From the spectral broadening at higher injection currents and the temperature tuning coefficient derived in the following paragraph, we were able to estimate the temperature increase during the pulse to be on the order of 20 - 30 K. Another possible reason for the spectral broadening at higher current levels is the onset of lasing in higher order lateral modes in these gain-guided structures. This explanation is supported by the fact that the L-I-curves show several kinks.

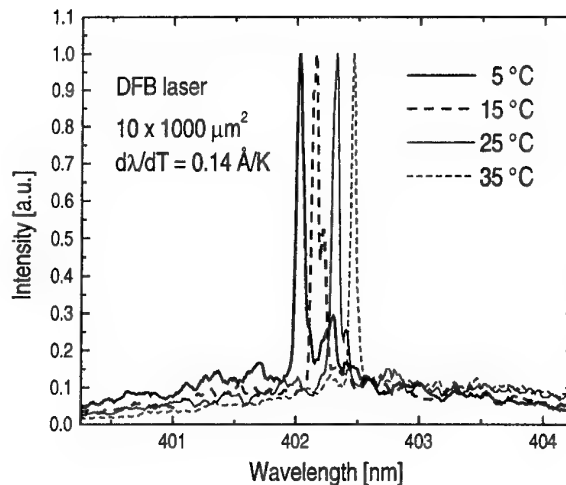


Fig. 2 - Emission spectra of the same device as in figure 1 at  $1.1 \times I_{th}$  and at different heat-sink temperatures. The temperature tuning coefficient obtained was 0.14 Å/K.

Emission spectra of a 1000  $\mu\text{m}$  long DFB laser at four different heat-sink temperatures are shown in figure 2; they reveal laser oscillation in a single longitudinal mode with a sidemode suppression ratio of 15 dB and at a center wavelength of around 402 nm. Given the grating period of 240 nm and the above emission wavelength, we were able to calculate the effective refractive index of the propagating mode to be  $n_{\text{eff}} = 2.52$ . In order to maintain narrow emission spectra for this measurement, we adjusted the injection current to always be at  $1.1 \times I_{\text{th}}$ . The device remained in a single mode for temperatures ranging from 2 °C to 35 °C, which is a temperature range of more than 30 K; the temperature tuning coefficient was on the order of 0.014 nm/K. For Fabry-Perot type lasers fabricated on the same wafer, we measured a much larger average temperature tuning coefficient of 0.065 nm/K.

### Quantum cascade DFB lasers at 10.16 $\mu\text{m}$

In this second part, we will report the fabrication of distributed feedback quantum cascade (DFB QC) lasers in the InGaAs/InAlAs material system, and also discuss very briefly

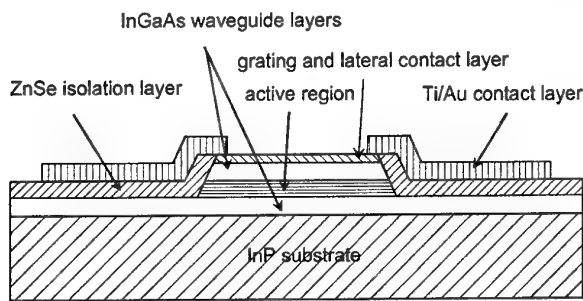


Fig. 3 – Schematic cross-section through a QC DFB laser without metal on top of the ridge waveguide.

including the creation of a photon, the electron makes a fast, because resonant, transition (under the help of an optical phonon) into the lowest energy level of the QW pair, and finally tunnels into the injector region of the next period. One electron is thus capable of producing many photons; which can result in quite high quantum efficiencies and remarkably high output powers.

In order to be useful for gas sensing applications, it is necessary to operate these lasers in a single longitudinal and transverse mode. This can be achieved by the use of distributed feedback. DFB quantum cascade lasers have already been

their potential applications in gas sensing systems [3]. The current state of the art in this rapidly evolving research area will be shown in a snapshot. Quantum cascade lasers currently cover a wavelength range from 3.6 to 17 microns, with CW operation at mostly low temperatures (50K) and pulsed operation at room temperature [4], [5]. Their fabrication relies on MBE growth of InGaAs/InAlAs superlattices with up to 40 periods. Each of these periods consists of an injector region which funnels electrons into the upper lasing level of a quantum well pair or triplett. After a vertical transition

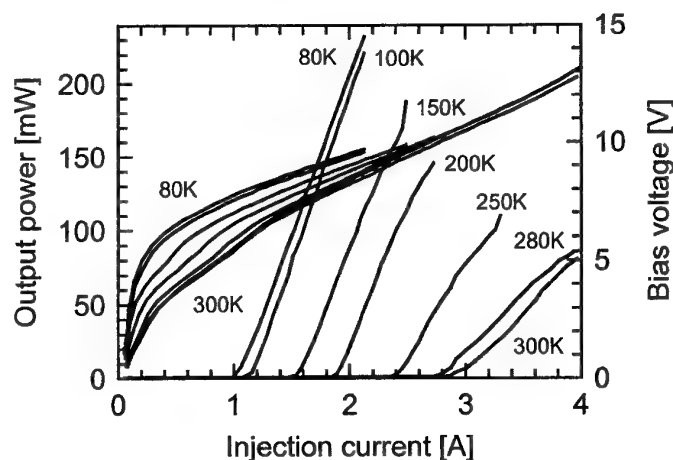


Fig. 4 – L-I-curves of a 45  $\mu\text{m}$  wide and 1 mm long QC-DFB laser operating at 10.16  $\mu\text{m}$ . All curves were measured under pulsed current injection.

demonstrated at wavelengths around 10 microns. However, their fabrication was rather sophisticated; it included a first epitaxial growth, etching of a grating, and following re-growth. For facilitating processing, it is advantageous to fabricate these devices without re-growth. This leads to a design with a grating which is exposed to air or the top metal. Since such a configuration normally causes high absorption losses, we used a lateral contact scheme without metal on top of the ridge waveguide. A schematical cross-section of such a laser is shown in figure 3. With a device of  $45\text{ }\mu\text{m}$  width and 1 mm length, we achieved an output power of 230 mW at 85 K and 80 mW

at 300 K. Corresponding L-I-curves are shown in figure 4. Within this same temperature range, the emission wavelength changed from  $996\text{ cm}^{-1}$  to  $982\text{ cm}^{-1}$ , as presented in figure 5. Also shown is a spontaneous emission spectrum of the same device measured at 85 K.

In conclusion, we have presented devices in two entirely different wavelength ranges, into which one got access recently by utilizing either new materials (for the short wavelength lasers) or intersubband transitions instead of intraband-transitions (for the mid-infrared quantum cascade lasers). While the short wavelength emitters will be used in optical data storage systems, mid-infrared QC lasers will have their main applications in environmental sensors. We showed also that the use of distributed feedback is of great importance for the QC-laser devices, while it offers an interesting fabrication alternative for InGaN/GaN-based short-wavelength lasers.

The authors would like to thank R.L. Thornton, R.M. Wood, M. Kneissl, C.J. Dunnrowicz, and N.M. Johnson from XEROX PARC for their assistance and encouragement in violet/blue laser fabrication. Likewise, the help and support of A. Müller, M. Beck, U. Oesterle, S. Blaser from Neuchâtel University are gratefully acknowledged.

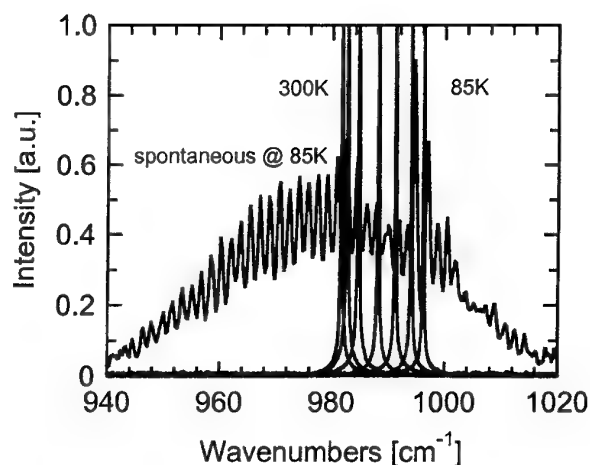


Fig. 5 – Emission spectra of a QC-DFB laser at different temperatures. The spontaneous emission spectrum was measured at 85 K.

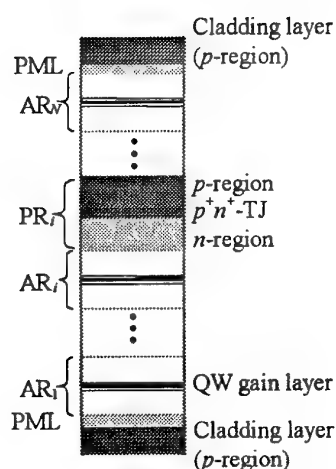
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## Tunnel-Junction-Connected Cascade Laser

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We describe a design of a bipolar cascade laser, which, in principle, is capable of high optical power emission in a narrow far-field output beam at currents comparable to those of a conventional laser. This cascade laser utilizes reverse biased  $p^+n^+$ -tunnel junctions for effective quasi-Ohmic connection between epitaxially stacked laser diodes. The proposed device consists of several double heterostructure laser diodes electrically connected in series

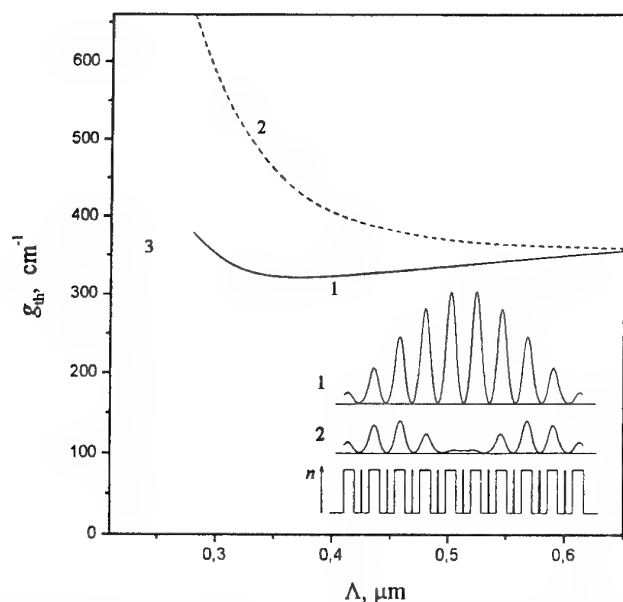


**Figure 1.** Model design of the tunnel-junction-connected edge-emitting laser.

by tunnel junctions (Fig. 1). The laser cavity consists of  $N$  GaAs active regions (high refractive index, narrow band-gap) separated by  $N-1$  wide-band-gap passive regions for carrier confinement. The passive regions are formed by  $p$ - and  $n$ -type AlGaAs injection regions that provide carrier injection into the adjacent active regions, and a GaAs  $p^+n^+$ -tunnel junction between them. Strong overall inter-element optical coupling is reached by shortening spatial period  $\Lambda$  of the structure. A small inter-element distance in the cascade structure does not obviously result in much worse threshold characteristics of the laser. Contrary, as we have shown for a particular structure of the cascade vertical-cavity surface-emitting laser [1, 2], the laser threshold can be comparable to that of a single-active-region surface-emitting laser. To prevent intensive absorption in the tunnel junctions we propose to match nodes of the optical field with positions of the tunnel junctions.

Optical losses in the inter-element regions suppress all but the out-of-phase mode. Concentrated losses, even very intensive as in the case of the tunnel junctions, can hardly affect the out-of-phase mode if they are in the mode's nodes, but, at the same time, they cause complete degradation of all other modes. Moreover, more intensive losses improve inter-modal discrimination. Thus, a cascade  $N$ -diode laser will operate in the out-of-phase mode of the order  $N$ . This mode has  $(N-1)$  zeros, which are aligned with  $(N-1)$  tunnel junctions, i.e. with the points of maximum losses.

Figure 2 shows dependence of the threshold gain,  $g_{th}$ , on the inter-element distance,  $\Lambda$ , in a ten-diode cascade lasers. If the tunnel junction is placed in the middle of the passive region, the threshold gain for the out-of-phase mode in the device remains almost the same or even decreases. The threshold for this mode gets growing when the mode becomes weakly confined due to shortening of the inter-element distance. For the ten-diode laser with 0.15- $\mu\text{m}$ -active regions, the optimal inter-element distance is about 0.36  $\mu\text{m}$ . The laser structure is characterized by a minimum threshold gain and high inter-modal selectivity:  $g_{th}=320 \text{ cm}^{-1}$  for the out-of-phase  $N$ -th mode compared to  $g_{th}=435 \text{ cm}^{-1}$  for the  $(N-1)$ -mode with  $(N-2)$  zeros. For a single-diode device with the same parameters but without tunnel junctions, the threshold



**Figure 2.** Threshold gain,  $g_{th}$ , for the out-of-phase  $N$ -th mode (curve 1) and  $(N-1)$ -mode (curve 2) as a function of inter-element distance,  $\Lambda$ , for a ten-diode cascade lasers with  $w_{AR}=0.15 \mu\text{m}$ . Curve 3 shows the threshold gain for single-element laser. The insert shows an index profile and field patterns for the corresponding modes.

complete transverse spatial coherence at current comparable to that of a conventional diode laser. Operating in the out-of-phase mode, the laser have predominantly two-lobed output beam with a far-field angular divergence of about  $\lambda/N\Lambda$  radians for each lobe. Accordingly, the photometric brightness of the laser scales with the number of cascaded diodes. Since the total power output of the  $N$ -diode cascade laser increases as  $N$ , and the angular beam divergence decreases as  $1/N$ , the photometric intensity or power per unit solid angle will be proportional to  $N^2$ .

gain would be  $340 \text{ cm}^{-1}$ . The optical-mode size in the vertical direction for this ten-diode laser,  $\approx 3.6 \mu\text{m}$ , is well matched to the in-plane width of a typical single-mode laser,  $\approx 4 \mu\text{m}$ . Provided that the power density where catastrophic facet damage occurs is about  $2.5 \text{ MW/cm}^2$  [3], the described laser can produce cw power output up to  $0.36 \text{ W}$ . However, the power output per laser diode would be only  $36 \text{ mW}$ , which means that dissipated power per laser diode and injection current will be comparatively small at critical conditions. Ultimately, this will result in longer lifetime of the device.

The proposed cascade laser is capable of high power, single-frequency and single-spatial mode operation, with

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# Low Avalanche Multiplication Noise in GaAs, GaAlAs and InP Sub-Micron PIN Diodes

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## Abstract

Measurements of avalanche excess noise factor  $F$  made on a range of homojunction GaAs, GaAlAs and InP  $p^+-i-n^+$  diodes with  $i$ -region widths  $w$  that range from  $\approx 1\mu\text{m}$  to  $0.05\mu\text{m}$  are presented. These show that for a given multiplication  $M$ , the excess noise factor monotonically decreases as  $w$  decreases. Moreover,  $F$  is always less than that predicted by the widely used theory due to McIntyre. Results from a Monte-Carlo transport model used to calculate  $F$  agree closely with the experimental data.

## 1. Introduction.

Recently, Levine [1] has calculated that avalanche photodetectors (APDs) with a gain-bandwidth product as high as 150GHz are possible in detectors having thin ( $< 0.3\mu\text{m}$ )  $i$ -regions. Hu [2] and Li [3] have shown that the avalanche excess noise factor  $F$  reduces monotonically in GaAs  $p^+-i-n^+$  APDs as the  $i$ -region decreases from  $1.0\mu\text{m}$  to  $0.05\mu\text{m}$ . Sub-micron III-V APDs thus merit further investigation.

## 2. Noise Measurements.

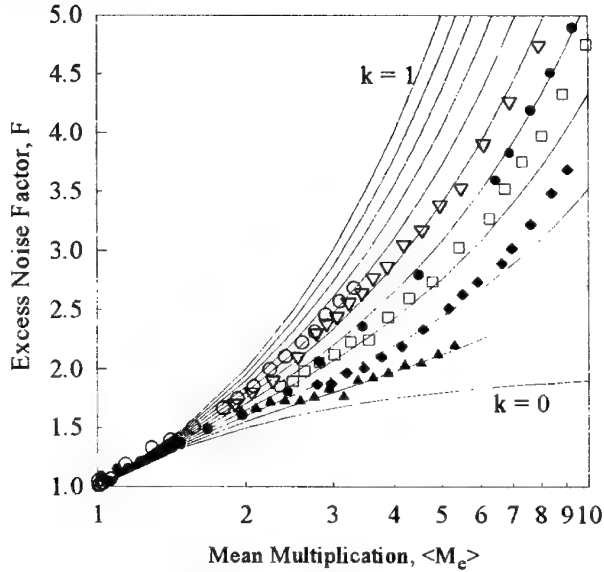


Fig.1: Excess noise factor for pure electron injection versus multiplication, for a range of GaAs  $p^+-i-n^+$  structures with nominal avalanche widths  $w=1.13\mu\text{m}$ ( $\circ$ ),  $w=0.57\mu\text{m}$ ( $\nabla$ ),  $w=0.31\mu\text{m}$ ( $\bullet$ ),  $w=0.20\mu\text{m}$ ( $\square$ ),  $w=0.10\mu\text{m}$ ( $\blacklozenge$ ),  $w=0.049\mu\text{m}$ ( $\blacktriangle$ ). Solid lines show McIntyre predictions with  $k=\beta/\alpha$  increasing from 0 to 1 in steps of 0.1.

Figs.1 shows the measured excess noise factor  $F$  for electron initiated multiplication versus multiplication  $M$ , in a number of GaAs  $p^+-i-n^+$  diodes having different  $i$ -region widths  $w$ . The solid curves are excess noise factor  $F$  predicted by McIntyre's theory [4] and are given by:-

$$F = kM + (2 - 1/M)(1 - k) \quad (1)$$

where  $k=\beta/\alpha$  if the initiating carriers are electrons or its reciprocal if they are holes. Here  $\alpha$  and  $\beta$  are the electron and hole ionisation coefficients respectively. For any given  $M$ , the experimental values of  $F$  are seen to fall as the  $i$ -region length  $w$  decreases. This is contrary to equation (1). To appreciate why, consider the case of the longest device ( $w=1.13\mu\text{m}$ ). The electric field in this sample is close to 300kV/cm, for which it is known that  $k \approx 0.6$  [5]. For the shortest device ( $w=0.05\mu\text{m}$ ) the field is in excess of 1000kV/cm and  $k$  is close to unity [5]. Thus, if McIntyre's theory were appropriate,  $F$  should increase as  $w$  grows smaller. But clearly from Fig.5 it moves in the opposite direction. Hole initiated ionisation in GaAs, and both electron and hole initiated ionisation in GaAlAs and InP, exhibit similar behaviour and these results will be presented.

## 3. Monte-Carlo Model

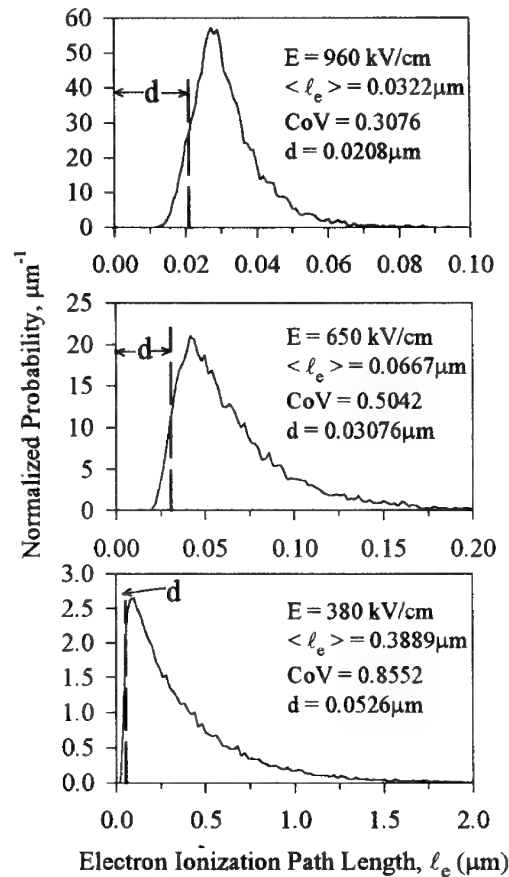


Fig.2: Probability distribution,  $P(l)$  for electron ionisation path lengths for  $E=380, 650$  and  $960$  kV/cm.

We have studied the distribution of path lengths required to achieve impact ionisation using Monte-Carlo

simulations to model the hot carrier transport [6]. By following many ionisation events for a given type of carrier and logging the path lengths  $l$  required to achieve ionisation into finely divided space bins, a histogram can be constructed. This histogram, in the limit of very narrow space bins, and appropriately scaled, is the probability distribution function (PDF) for impact ionisation path length, denoted by  $P(l)$ . Fig.2 shows  $P(l)$  for electrons, in three different electric fields typical of those in the experiments. Since  $P(l)\delta l$  is the probability that an electron will ionise in travelling a distance between  $l$  and  $l+\delta l$ , following a previous ionisation, the area under all these curves must be unity. Also shown for each PDF is the mean value of the ionisation path length  $\langle l \rangle$  and the coefficient of variation (CoV). The former is just the reciprocal of the electron ionisation coefficient  $\alpha$  at the field concerned and the latter is the ratio of the standard deviation in  $l$  to its mean  $\langle l \rangle$ ; it forms a convenient measure for the fractional spread of the distribution function. The dead space  $d=W_i/qE$  is also noted. This is the distance an electron would have to travel ballistically in the field  $E$  in order to achieve the ionisation threshold energy  $W_i$ . A value of 2eV is assumed here.

The general shapes of all the PDFs shown in Fig.2 are similar. The curves start to rise from zero for values of ionisation path length slightly less than the corresponding dead space  $d$ . For a carrier to achieve impact ionisation in a distance less than  $d$  it has either to absorb more phonons than it emits or more commonly, have some field-directed energy from its previous ionising collision. The overwhelming majority of carriers that impact ionise experience a path length longer than the dead space as they struggle against phonon scattering to gain the necessary threshold energy.

We immediately note from Fig.2 that at the lowest field shown of 380 kV/cm, the PDF closely resembles a simple exponentially decaying function. Its CoV is 0.86 which is the largest of the three shown. An exact exponential, with no dead space, has a CoV of unity. As the electric field is increased the CoV is seen to become smaller and transport is increasingly ballistic. The fractional spread in ionisation path length is less, thus impact ionisation becomes more deterministic. The PDFs for holes show the same sort of field dependency. Since McIntyre's expression for noise figure, equation (1), implicitly assumes that the PDFs for both electron and holes have a simple exponential form, it is not surprising therefore that it overestimates the excess noise, particularly in short devices.

#### 4. Determination of the Excess Noise Factor.

The excess noise figure due to avalanche multiplication is given by:-

$$F = \langle M^2 \rangle / \langle M \rangle^2 \quad (2)$$

where  $\langle M \rangle$  is the mean multiplication per injected carrier and  $\langle M^2 \rangle$  is the mean square value. To evaluate  $F$  for electron (hole) initiated multiplication, an electron (hole) is injected with small momentum from one edge of the

multiplication region. The motion of the primary initiating carrier and of the electrons and holes generated subsequently are followed using the Monte-Carlo simulation described earlier. The total number of ionisation events  $N_T$  is recorded when all carriers have left the multiplication region; the multiplication for that trial is  $M = N_T + 1$ . By repeating the procedure for many trials,  $\langle M \rangle$  and  $\langle M^2 \rangle$  and hence  $F$  can be calculated. Between  $10^3$  and  $10^4$  trials are needed for convergence.

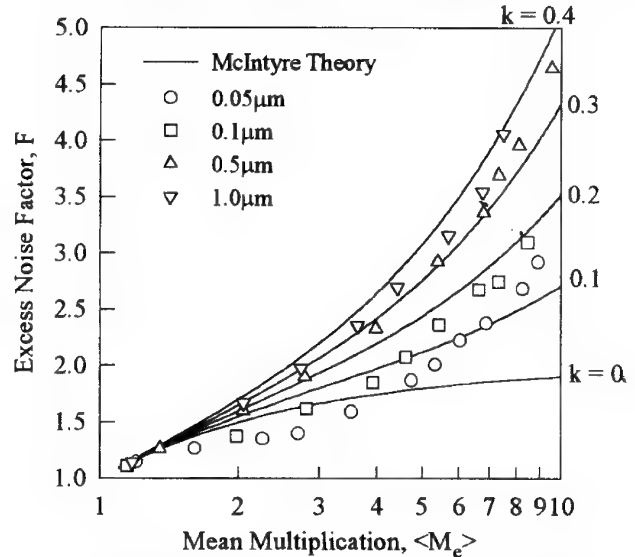


Fig.3: Excess noise factor versus mean multiplication for electron injected multiplication in ideal PIN GaAs diodes. Solid lines depict the results of McIntyre's theory for different values of  $k$  and symbols denote values calculated from the MC model.

Fig.3 shows the values of  $F$  versus  $\langle M \rangle$  calculated as outlined above, for a range of devices with similar i-region lengths as those measured experimentally. These demonstrate the same trends as the experimental data in Fig.1 but generally predict slightly lower noise figures than measured.

#### 5. Conclusions

The experimentally measured excess noise factors for a range of III-V  $p^+-i-n^+$  APDs with sub-micron i-region widths are lower than predicted by the widely used theory of McIntyre. This has been explained with the help of Monte-Carlo simulations.

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# High Efficient $\text{Al}_{0.1}\text{Ga}_{0.9}\text{As}$ Solar Cells

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## Abstract

Photovoltaic devices of high efficiency are based on Si and III-V semiconductor technologies. AlGaAs grown on Si substrate is among the most important material candidate for optoelectronic circuitry as well as for solar applications. Therefore, an attempt is made in order to examine such cells. In this work both the emitter and base regions are considered in order to find the optimized device makeup such as the semiconductor layer thickness and impurity doping concentration. An Am1.5G of 24.74 % has been obtained.

## Introduction

Photovoltaic devices of high efficiency are based on Si and III-V semiconductor technologies. The main aim of the several simulations, theoretical or experimental researches is to improve conversion efficiency advanced technology. Since the ternary alloy AlGaAs grown on Si substrate is among the most important material candidate for optoelectronic circuitry as well as for solar applications [1] and is specially of considerable interest for multispectral applications [2]. This paper describes a study of an  $\text{Al}_{0.1}\text{Ga}_{0.9}\text{As}$  solar cell. The aim of this work is to find the optimized device makeup such as the semiconductor layer thickness and impurity doping in emitter and base regions. The optimal emitter thickness and doping as well as the base thickness and doping are calculated by 1-dimensional computer program PC1D [3]. All calculations are performed assuming a 3% loss due to the shadow and reflection. Figure 1 shows the schematic cross-sectional view of  $\text{Al}_{0.1}\text{Ga}_{0.9}\text{As}$  solar cell.

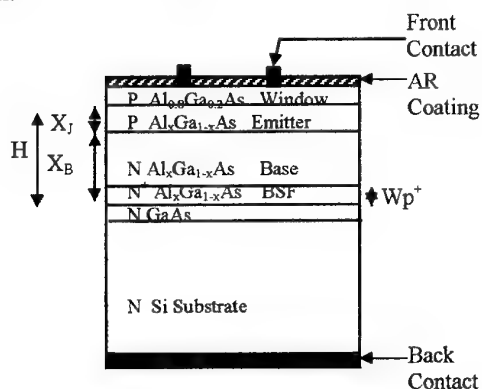


Fig.1.  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  solar cell structure.

## Results and discussion

The results were generated for 0.25  $\text{cm}^2$  area with an Erfc emitter profile. A front surface recombination

velocity  $S_{\text{front}}$  of  $1.10^4$  cm/s is adopted here (The window is not accounted in the modeling.). For the back surface recombination velocity  $S_{\text{back}}$  a value of  $1.10^7$  cm/s for an Ohmic contact is used and a value of  $1.10^4$  cm/s for a BSF layer.

First, the cell performance as a function of the base device makeup is calculated using a heavily doped and thin emitter ( $N_A=5 \times 10^{18} \text{ cm}^{-3}$  and  $x_j=0.5 \mu\text{m}$ ). The cell thickness  $H$  is varied in the range of  $[3-20 \mu\text{m}]$  for different concentrations  $N_D$  in the base ( $5 \times 10^{14} \text{ cm}^{-3} - 5 \times 10^{17} \text{ cm}^{-3}$ ).

Figure 2 illustrates the dependence of the conversion efficiency of the cell on the base device makeup. The variation of the conversion efficiency versus the base thickness for different concentrations presents a slight increase until  $4.5 \mu\text{m}$  then becomes constant. The saturation observed for thickness more than  $5 \mu\text{m}$  is due to the fact that carriers are generated at the front surface.

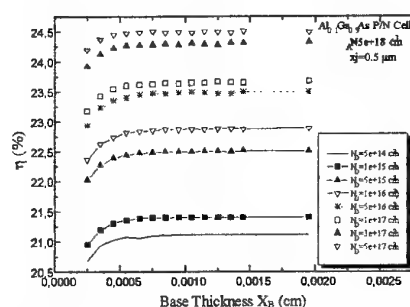


Fig.2. Dependence of the conversion efficiency of the cell on the base device makeup.

The conversion efficiency increases if the base doping level increases. This is due to the fact that the conversion efficiency improves with decreasing base resistivity.

In other hand, the high base doping level degrades slightly the quantum efficiency in the long wavelength region. This is the result of the degradation of the short

circuit current in this region. Indeed, the increase of the base doping level shift a part of the space charge region in the front region which is artificially reduced. Also, the quantum efficiency in the long wavelength region depends especially on the lifetime and diffusion length in the base.

This degradation is compensated with the presence of a back electric field. BSF structure is a technique which improves the quantum efficiency in this region (see fig.3).

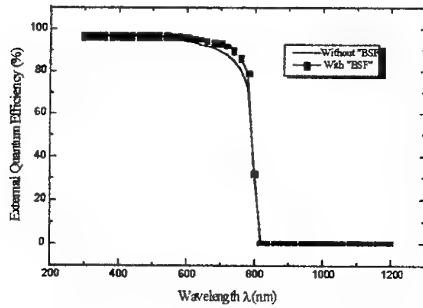


Fig. 3. BSF effect on the quantum efficiency.

The slight compensation in the quantum efficiency is reflected in the parameters values of table 1. Because a back electric field effect is more apparent when thickness is reduced.

|          | Jcc (mA/cm <sup>2</sup> ) | Vco (V) | FF (%) | η (%) |
|----------|---------------------------|---------|--------|-------|
| Sans BSF | 30.656                    | 1.149   | 86.36  | 22.48 |
| Avec BSF | 31.272                    | 1.155   | 86.1   | 23.00 |

Table 1. Photovoltaic characteristics of the p<sup>+</sup>n and p<sup>+</sup>nn<sup>+</sup> Al<sub>0.1</sub>Ga<sub>0.9</sub>As solar cells under AM0 conditions.

It can be pointed out that a 4 μm thick with a base doped at  $N_D = 5 \times 10^{17} \text{ cm}^{-3}$ , a BSF layer of 2.6 μm thick and doped at  $3 \times 10^{18} \text{ cm}^{-3}$  will yield a maximum efficiency provided  $N_A = 5 \times 10^{18} \text{ cm}^{-3}$  and  $x_j = 0.5 \mu\text{m}$ .

In optimizing the emitter device makeup the optimized base is used. The concentration varies in a range of  $[1 \times 10^{18} \text{ cm}^{-3} - 5 \times 10^{19} \text{ cm}^{-3}]$  and emitter depth in the range of  $[0.01 \mu\text{m} - 3 \mu\text{m}]$ .

The conversion efficiency decreases strongly with both the junction depth increase and doping level above  $5 \times 10^{18} \text{ cm}^{-3}$ , value at which it shows the best qualities. The conversion efficiency is seen to be constant for values below 1.25 μm at that doping (see fig.4).

The conversion efficiency decreasing with increasing junction depth may be understood as minority carrier lifetime in Al<sub>0.1</sub>Ga<sub>0.9</sub>As is small (<10 ns). Therefore, carriers generated at the front surface of solar cell structure may not reach the pn junction if the emitter thickness is larger compared to the diffusion length. This result is supported by other researches [4]. Moreover, the quantum efficiency depends on the front surface recombination velocity and the lifetime in the emitter. Furthermore, the degradation in quantum efficiency in

short wavelength region shown in figure 5 at high doping levels is attributed to the bandgap narrowing, which permit a strong absorption of photons by the free carriers.

Consequently,  $N_A = 5 \times 10^{18} \text{ cm}^{-3}$  as an emitter doping and a junction depth  $x_j$  of 0.35 μm are adopted.

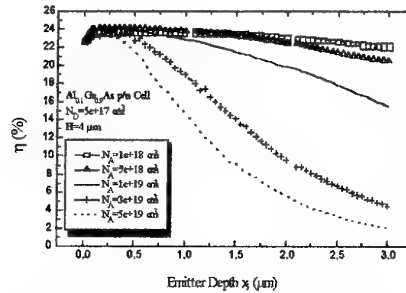


Fig.4. Dependence of the conversion efficiency of the cell on the emitter device makeup.

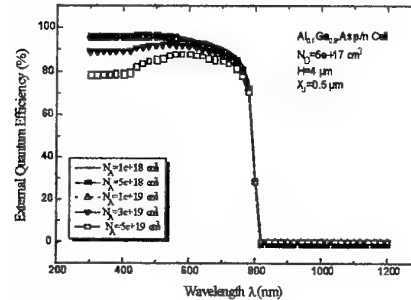


Fig. 5. Emitter doping effect on the quantum efficiency.

## Conclusion

In conclusion, the physical and technological parameters of the cell are  $H = 4 \mu\text{m}$ ,  $x_j = 0.35 \mu\text{m}$ ,  $W_p^+ = 2.6 \mu\text{m}$ ,  $N_A = 5 \times 10^{18} \text{ cm}^{-3}$ ,  $N_D = 5 \times 10^{17} \text{ cm}^{-3}$  and  $N_D^+ = 5 \times 10^{17} \text{ cm}^{-3}$ . These allow an AM1.5G efficiency of 24.74 %. This cell can be used in a multispectral applications.

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Wednesday, May 26, 1999 14:00

## Reliability and Noise

- *Hot electrons and reliability in HEMTs (invited paper)* p. 39  
 Enrico Zanoni, G. Meneghesso, D. Buttari, M. Maretto, and G. Massari  
 University of Padova, Padova, Italy
- *Comparison of the electrostatic discharge sensitivity of 1300nm lasers and light emitting diodes* p. 43  
 H.C. Neitzert and A. Piccirillo  
 Centro Studi e Laboratori Telecomunicazioni (CESLT), Torino, Italy
- *Reliability evaluation of GaAs HBT Technologies* p. 45  
 C. Maneux, N. Labat, N. Saysset, A. Touboul, Y. Danto, JM. Dumas<sup>(1)</sup>, M. Riet<sup>(2)</sup>, and A. Scavennec<sup>(2)</sup>  
 University of Bordeaux-IXL, Talence, France  
<sup>(1)</sup> University of Limoges-ENSIL, Limoges, France  
<sup>(2)</sup> OPTO+/CNET, Marcoussis, France
- *Three-terminal off-state breakdown in AlGaAs/GaAs power HFETs : a temperature-dependent analysis of the gate reverse current* p. 47  
 D. Dieci, P. Cova<sup>(1)</sup>, R. Menozzi<sup>(1)</sup>, C. Lanzieri<sup>(2)</sup>, G. Meneghesso<sup>(3)</sup>, and C. Canali.  
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<sup>(2)</sup> Alenia systems, Roma, Italy  
<sup>(3)</sup> University of Padova, Padova, Italy
- *Electroluminescence of composite channel AlInAs / InGaAs / InP / AlInAs HEMTs* p. 49  
 N. Cavassilas, F. Aniel, P. Boucaud, R. Adde, H. Maher<sup>(1)</sup>, J. Décobert<sup>(1)</sup>, and A. Scavennec<sup>(1)</sup>  
 University of Orsay-IEF, Orsay, France  
<sup>(1)</sup> OPTO+/CNET, Marcoussis, France
- *Influence of deep levels in InAlAs/GaInAs/InP HFETs* p. 51  
 A. Souifi, B. Georgescu, G. Brémont, M. Py<sup>(1)</sup>, J. Décobert<sup>(2)</sup>, G. Post<sup>(2)</sup>, and G. Guillot  
 LPM-INSA, Lyon, France  
<sup>(1)</sup> EPFL, Lausanne, Switzerland  
<sup>(2)</sup> OPTO+/CNET, Marcoussis, France
- *Low frequency noise comparison between InP/InGaAs and Si/SiGe heterojunction bipolar transistors* p. 53  
 S.G. Jarrix, C. Delseny, A. Penarier, F. Pascal, S. Blayac<sup>(1)</sup>, and P. Llinares<sup>(2)</sup>  
 University of Montpellier-CEM2, Montpellier, France  
<sup>(1)</sup> OPTO+/CNET, Marcoussis, France  
<sup>(2)</sup> ST Microelectronics, Crolles, France
- *Interwell-transfer noise in InP-based InGaAs channels caused by electron tunneling at equilibrium and low electric fields* p. 55  
 A. Matulionis, V. Aninkevicius, and J. Liberis  
 Semiconductor Physics Institute, Vilnius, Lithuania

## Hot Electrons and Reliability in HEMTs

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The renovated interest in the study of hot carrier phenomena in III-V FET devices originates from two main motivations: (i) the quest for higher on- state and off-state device breakdown voltages, which limit the maximum operating voltage of the devices; (ii) the need for an improved understanding of reliability problems due to hot carrier effects, which may lead to parametric degradation or burn-out phenomena. For III-V devices, the relevance of these phenomena, which were already well known for Si MOSFETs, was recognized at the beginning of this decade [1],[2]; in the following years, specific electrical measurements and electroluminescence techniques have been implemented and applied to the experimental characterization of hot carrier phenomena in MESFETs and HEMTs [3],[4]; standard reliability "life" tests have been modified in order to include "hot-electron" tests [5]; complex physical models have been developed in order to take into account impact-ionization phenomena and related effects [6].

Although there is no general agreement on breakdown definitions, testing methods and, sometimes, even on the interpretation of physical phenomena involved in breakdown or in hot-carrier degradation, our insight in these phenomena has significantly improved in the last ten years. From the practical point of view, one could desire the availability of :

(i) simple electrical measurements enabling the identification of the onset of hot carrier phenomena, the definition of off-state and on-state breakdown, the comparison of different device structures.

For sake of simplicity, these should be DC measurements, achieved by means of a standard curve tracer. Gate current measurements are usually adopted to this purpose [7,8], see Fig. 1. Breakdown is defined as the locus of  $V_{DS}$ ,  $I_D(V_{GS})$  values which correspond to a pre-defined gate current density (usually 1 mA/mm of gate width). By driving the device at constant gate current the measurements (of both off- and on- state breakdown, [9,10]) can be carried out in well controlled and reproducible conditions, avoiding device damage, see Figs 2 and 3.

(ii) pulsed electrical measurements allowing one to avoid parasitic phenomena due to device self-heating, and to study breakdown in a more realistic and non-destructive way.

Transmission Line Pulse techniques, as suggested in [11] appear the most promising tool for the experimental evaluation of actual breakdown phenomena. TLP allows one to observe the snap-back of I-V characteristics and the large increase in the drain current consequent to on-state breakdown in a non destructive way and avoiding self-heating effects, see Figs.3,4.

(iii) experimental techniques capable of providing information on hot carrier transport phenomena, parasitic bipolar effects, and on anomalies such as current crowding and "hot spots".

Light emission measurements, i.e. spectroscopic analysis of electroluminescence and light emission imaging by means of an "emission" microscope are powerful tools from this point of view [4,12], see Fig. 5.

(iv) accelerated testing techniques which should be at the same time simple to carry out - and this usually means DC tests - and representative of device applications - which, on the contrary, would favour rf device testing.

Degradation due to hot carriers has been observed after rf accelerated testing, but there is at the moment no guideline for the correlation between DC and rf testing conditions, and very few [13] rules on the extrapolation of accelerated test lifetimes to field operating conditions.

(v) a set of reasonable failure criteria and a way to identify failure modes typical of hot-electron degradation, which usually consists in threshold voltage shifts, increase in drain parasitic resistance,

development of kink effects, increase in frequency dispersion of transconductance, appearance of peaks in Deep Level Transient Spectroscopy (DLTS) spectra [14], see Figs 6 and 7.

(vi) failure analysis techniques capable of detecting the mechanisms physically responsible for the degradation. Despite it is clear that hot-electron degradation often consists in the creation of deep levels at the device surface or at interfaces, see Fig. 7, and that this mechanism depends on surface treatments, passivation, technological steps adopted to obtain the gate recess and epitaxial technique etc., the actual mechanisms involved are still unknown.

On the other hand, from the point of view of the understanding and modeling of hot carrier and impact-ionization phenomena, we need:

(vii) accurate physical modeling of carrier transport and hot carrier effects, including impact-ionization. Advanced Monte Carlo simulators are available, which can describe the dynamics of breakdown effects and identify the role of generated holes in triggering parasitic bipolar effects eventually leading to breakdown, see Figs. 8 and 9.

(viii) compact, SPICE-like models capable of describing correctly gate current and breakdown conditions.

Most of these techniques are now available in several research laboratories, even if a unified view of breakdown phenomena is still lacking. The talk will overview main results obtained during the last few years, and will underline open questions, which still hinder the fabrication of high voltage, high power compound semiconductor HEMTs.

*We gratefully acknowledge C. Canali and F. Fantini (University of Modena), R. Menozzi, M. Manfredi and M. Pavesi (University of Parma), G. Vannini and A. Cavallini (University of Bologna) for useful discussion and exchanging data. Work partially supported by the European Research Office of the US Army Army (C.N 68171-98-M-5803), by CNR Italy P. F. MADESS II and by MURST Italy, 40%.*

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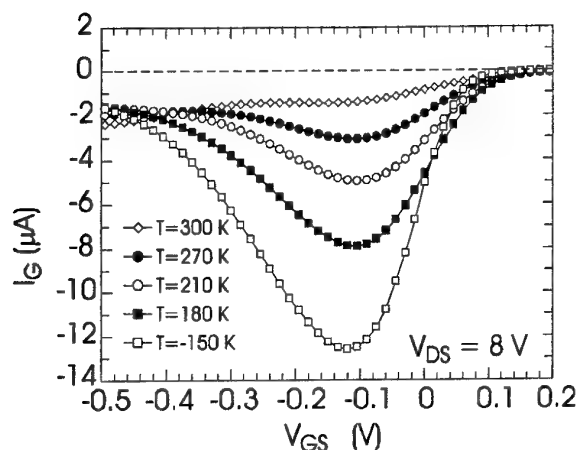


Fig.1  $I_G$  vs  $V_{GS}$  in a pseudomorphic AlGaAs/InGaAs HEMT. Gate current increases (in absolute value) at lower temperatures due to the increase of impact ionization

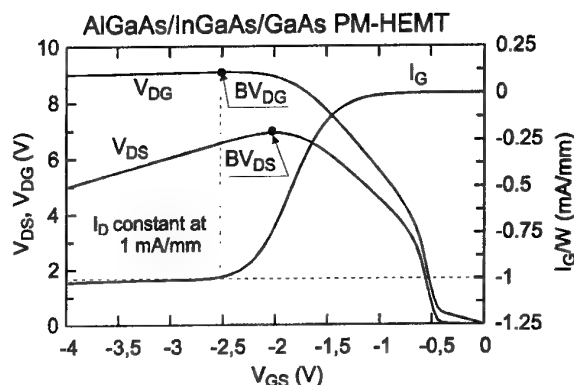


Fig. 2. Off-state breakdown measurements in a pseudomorphic HEMT according to [9].

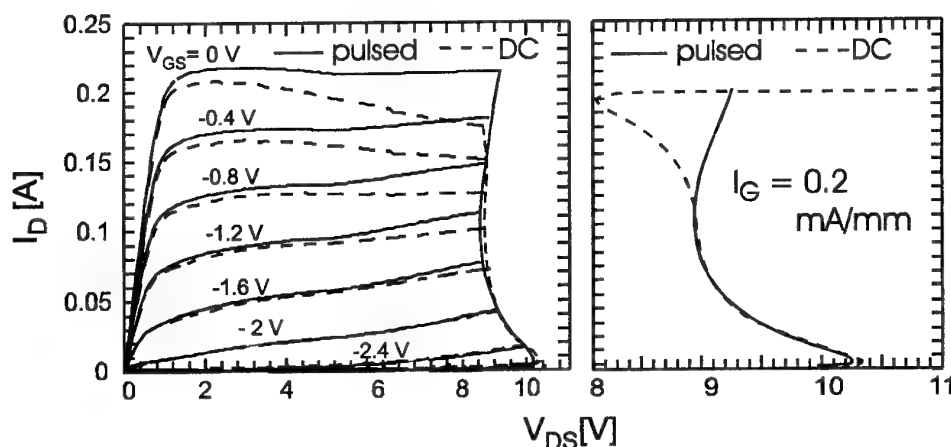


Fig. 3. Left: pulsed and DC  $I_D$  vs  $V_{DS}$  in a commercially available GaAs MESFETs. Curves are truncated by the by the  $I_D$ - $BV_{DS}$  locus at constant  $I_G = -10 \mu A$ , extrapolated from the  $I_G$  vs  $V_{GS}$  characteristics (not shown). This defines on-state breakdown. Right: pulsed and DC  $I_D$ - $BV_{DS}$  locus at constant  $I_G = -10 \mu A$ . Thermal effects are evident in DC measurements.

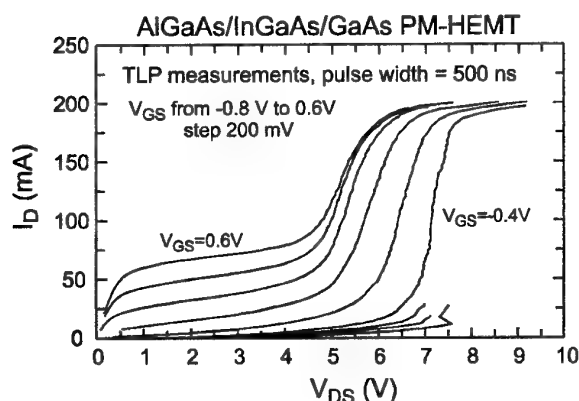


Fig.4. Transmission Line Pulse measurements of on-state breakdown in a pseudomorphic HEMTs.

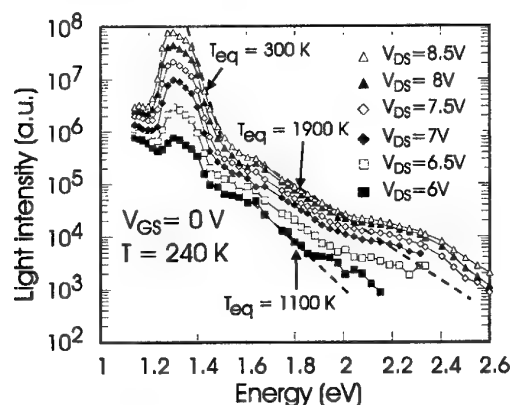


Fig.5 Emitted light intensity measured as a function of energy at  $T = 240 K$  for various  $V_{DS}$  and at  $V_{GS} = 0 V$  in a AlGaAs/InGaAs pseudomorphic HEMT.

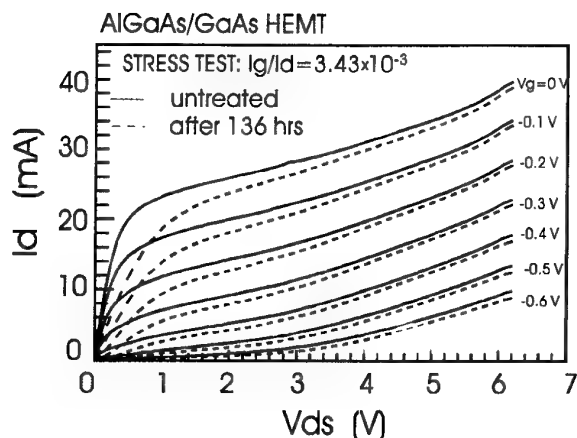


Fig. 6. Output characteristics measured in a device before any stress (solid line) and after 162 hrs of stress at  $V_{DS} = 6.2$  V,  $V_{GS} = -0.76$  V.

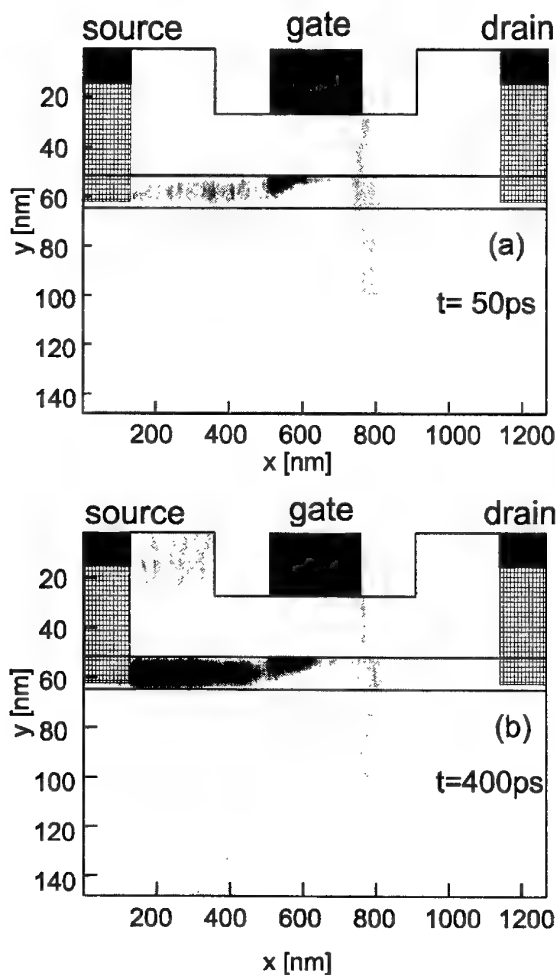


Fig. 8 Monte Carlo simulation of the hole density at two time values after switching-on of the impact ionization ( $V_{DS} = 8$  V,  $V_{GS} = -0.2$  V,  $T = 300$  K).

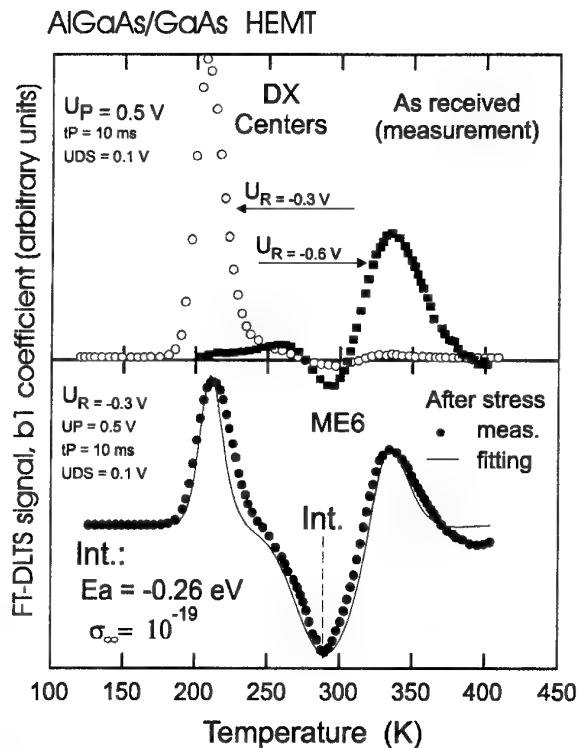


Fig. 7. Drain Current FT-DLTS measurements in an as received device and in a device after after 162 hrs of stress at  $V_{DS} = 6.2$  V,  $V_{GS} = -0.76$  V.

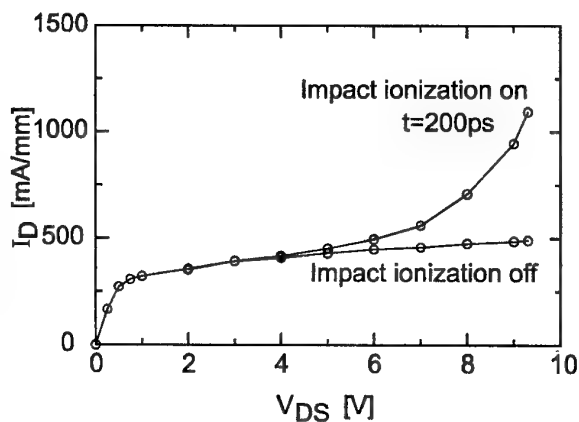


Fig. 9 Monte Carlo output current simulation at  $V_{GS} = -0.2$  V with and without impact-ionization taking into account (in an AlGaAs/InGaAs pseudomorphic HEMT).

## Comparison of the electrostatic discharge sensitivity of 1300nm lasers and light emitting diodes

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The electrostatic discharge sensitivity of Fabry-Perot (FP) laser diodes and light emitting diodes (LED) operating at a wavelength of 1300nm has been investigated. For each emitter type commercial devices from three different manufacturers have been tested, monitoring continuously electrical and optical properties of the devices during the step stress tests.

In the case of two types of the Fabry-Perot laser diodes we found - as commonly reported in literature [1,2] - rather high values of the forward bias ESD degradation threshold (>13000V) and much lower reverse bias values (>550V). In general a simultaneous degradation of the electrical diode characteristics and of the optical emission characteristics has been observed. In the case of one laser diode degraded under forward bias ESD stress we observed a significant spectral width reduction with single mode emission and a side-mode suppression of 28dB combined with a slight blue shift of the emission wavelength (see Fig.1), as reported in literature after the intentional introduction of mechanical defects [3,4]. The spectrum after degradation has the typical form as obtained with a cleaved coupled cavity structure.

The third Fabry-Perot laser type (ridge structure) exhibited degradation of the optical power without any significant modification of the electrical characteristics under forward bias already for pulse amplitudes exceeding 1000V. The reverse bias ESD degradation threshold for this type of laser was 2000V. It may be interesting to note that a 1300nm distributed feedback laser from the same manufacturer, with otherwise very similar diode structure as the Fabry-Perot laser, did not degrade during forward bias stress up to ESD pulse amplitudes of 9000V. Therefore we conclude that the low ESD damage threshold pulse amplitude in this Fabry-Perot laser is due to optical facet degradation. Threshold values for ESD induced degradation of the three different types of 1300nm light emitting diodes were between 5600V and 10000V under forward bias and between 1000V and 6500V under reverse bias.

In most cases after LED degradation only a parallel shift of the optical power versus bias current (P-I) characteristics to slightly higher current values has been observed without significant decrease of the differential quantum efficiency (Fig.2a). In the case of the Fabry-Perot lasers we observed either a large threshold current increase combined with a decrease of the differential quantum efficiency (Fig.2b) or a complete suppression of lasing after ESD pulse application with pulse amplitude above degradation threshold.

Besides measuring the reverse dark current at a given bias voltage and the optical power emitted at a given bias current, we monitored also the light pulses emitted during forward bias ESD stress ( see also [2,5] ). It has been found that in most cases continuous monitoring as well of the light pulse amplitude and of the decay time of the optical pulses enables an *in-situ* detection of the ESD degradation threshold pulse amplitude without time consuming measurements of the I-V and P-I characteristics after each ESD pulse.

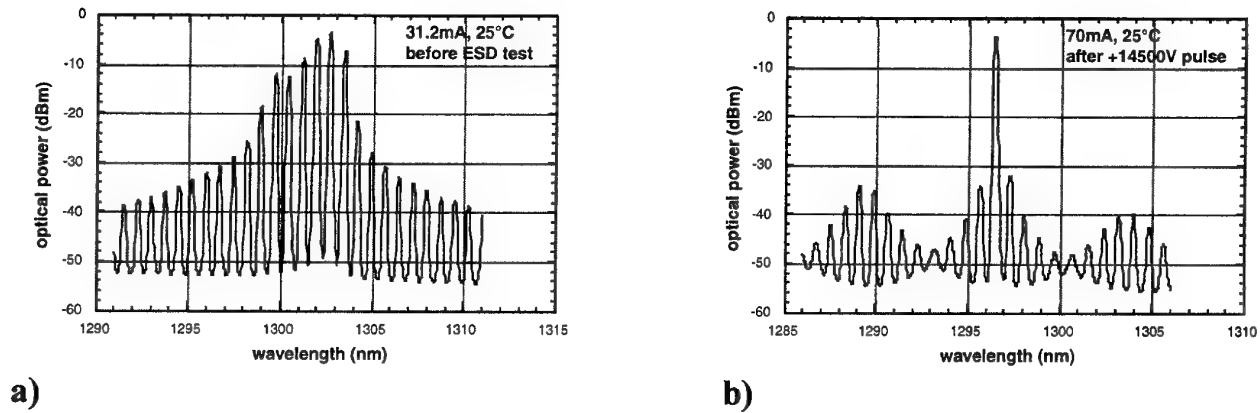


Fig.1 Optical spectrum of a Fabry-Perot laser diode a) before and b) after forward bias ESD stress

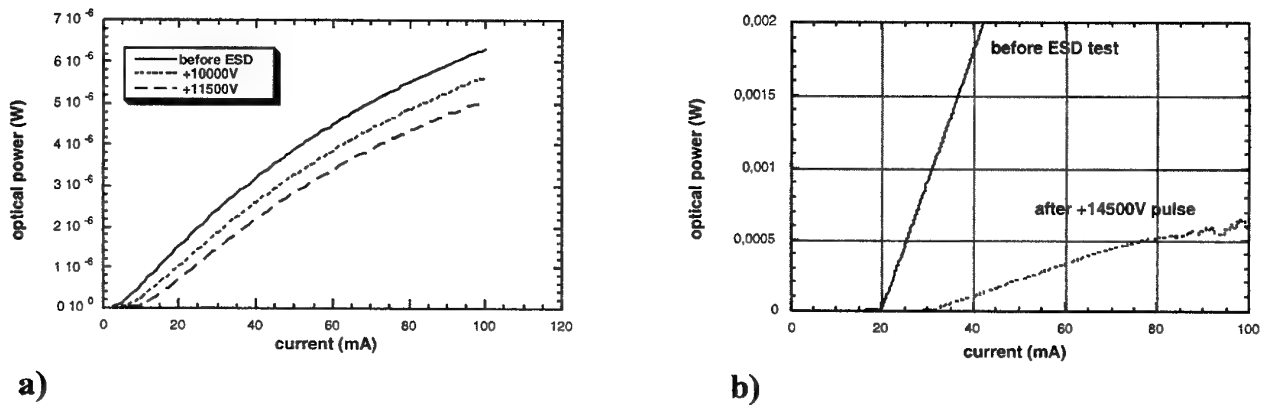


Fig.2 P-I characteristics of a) a 1300nm LED and b) a 1300nm Fabry-Perot laser diode before and after forward bias ESD stress

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# RELIABILITY EVALUATION OF GaAs HBT TECHNOLOGIES

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**Abstract** : This work presents an experimental procedure to evaluate the reliability of GaAs HBT based on the separation of ageing test accelerating factors applied on two test structures : HBT and TLM. To identify the physical origin of the degradation mechanisms, physical techniques are involved: EDX analysis, SEM and TEM observation. Three different manufacturing processes have been tested. The investigations reveal two major failure mechanisms.

## INTRODUCTION

Recent works on long-term stability of HBT electrical performances reveal the concerns associated with its reliability. Indeed, various laboratories have reported a wide range of activation energies and their projected lifetime [1] [2] [3]. To obtain deeper insight into failure mechanisms which limit HBT performances, we have implemented a specific life-test stress procedure to discriminate failure mechanisms accelerated either by temperature or by current-bias.

## DESCRIPTION OF DEVICES UNDER TEST

Devices under test were fabricated from three different epilayer wafers. Type #a HBT epitaxial structure has been grown by MOCVD whereas the types #b and #c epitaxial structures by CBE. In the three structures, Silicon and Carbon are the n-type and p-type dopant, respectively. The main features are detailed in figure 1.

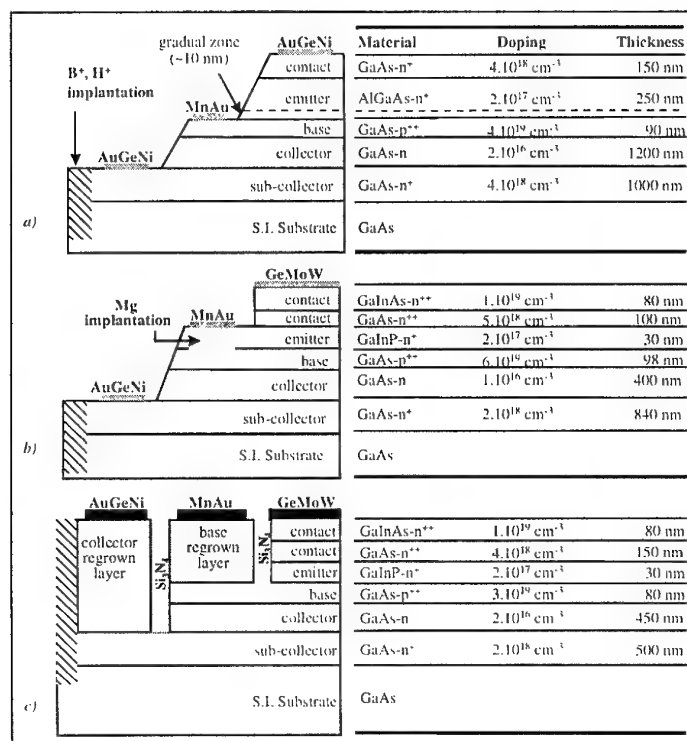


Figure 1 : Schematic cross section of the three technologies

## EXPERIMENTAL PROCEDURE

Because GaAs HBT failure mechanisms are not yet fully identified and might have different acceleration factors [4], a specific matrix approach has been set-up to separate the physical origin of the degradation :

- at wafer level, TLM structures and HBT have sustained high temperature burn-in at 220°C. TLM structures are used to characterize the collector, base and emitter layers. Then, the evolution of TLM resistance is compared with the evolution of HBT dc characteristics to evaluate the impact of HBT ohmic contact resistance shift on its operation.
- some transistors have been submitted to life-test under combined temperature and bias stresses (110°C oven temperature, forward base current density of 5x10<sup>3</sup> A/cm<sup>2</sup> and 1 V for collector-emitter voltage). The dc characteristics evolution is monitored and analysed on the basis of the HBT modified Gummel-Poon model parameters.

## EXPERIMENTAL RESULTS

The life-tests under high temperature stress have revealed metallurgical degradations while stress under bias and moderate temperature conditions have rather induced interface degradations :

- at high temperature, AuGeNi interdiffusion leads to a 12% increase of the AuGeNi contact resistance on n-type GaInAs and GaAs, regrown collector and subcollector layers, respectively,
- low temperature and bias stresses induce the migration of metallic species from the base contact towards the extrinsic base, leading to a decrease of the base-to-emitter leakage resistance of type #a and #c technologies. The same life-test applied to type #b technology does not induce similar degradation. It appears that the remaining GaInP emitter layer improves the stability of extrinsic surface base. However, type #b and #c technologies present Ge/Mo/W piling detachment from GaAs leading to an increase of the emitter series resistance.

| Technology Type | # a   | #b                                | #c  |
|-----------------|---|-----------------------------------|---|
| Detection       | Very low injection level  | High injection level              | Very low and high injection level   |
| Analysis        | EDX Analysis<br>MET Observation                                   | MEB Observation                   | EDX Analysis<br>MEB Observation   |
| Physical Origin | Lateral migration of base contact metallurgy : MnAu/Ti/Au on GaAs | Piling of Ge/Mo/W emitter contact | Lateral migration of base contact metallurgy MnAu/Ti/Au and Piling of Ge/Mo/W emitter contact |

Table 1 : Degradation mechanisms of the three technologies submitted to bias stresses

EDX analysis [5] and TEM observations (figure 2) have confirmed the lateral migration of the base contact metallurgy MnAu/Ti on GaAs and SEM observations (figure 3) have revealed the piling of Ge/Mo/W emitter contact [6].

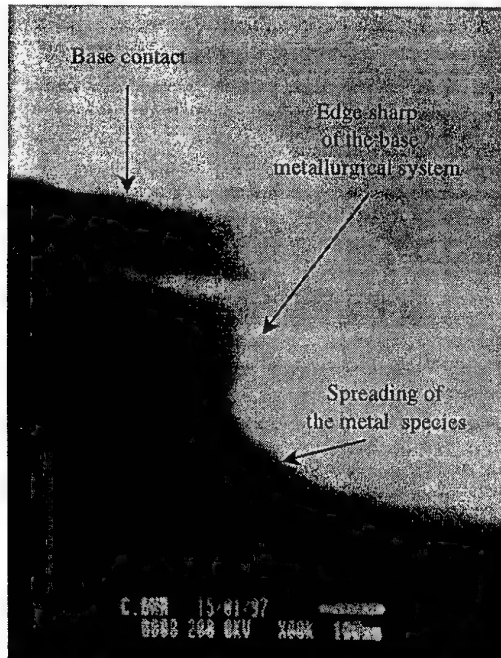


Figure 2: TEM Observation of the MnAu/Ti/Au ohmic contact on base layer near the extrinsic base

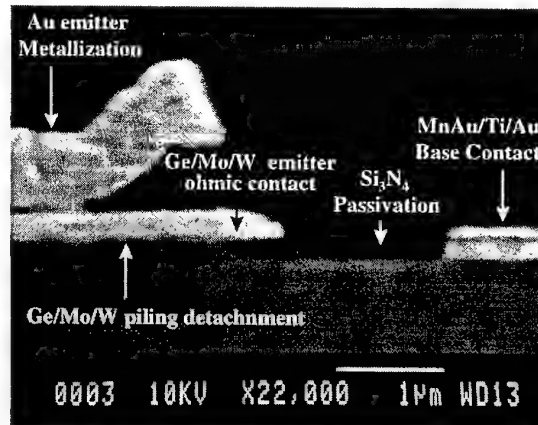


Figure 3: SEM observation of emitter ohmic contact

## CONCLUSION

We have shown that different HBT failure mechanisms are induced by high temperature storage and bias stress. The different failure accelerating factors in HBT justify the implementation of a life test strategy which stress conditions should be extrapolated to the field operating conditions.

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## Three-terminal off-state breakdown in AlGaAs/GaAs power HFETs: a temperature-dependent analysis of the gate reverse current

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The physical phenomena underlying the drain-gate breakdown of heterostructure FETs for microwave power applications are still not completely understood. On the other hand, power FETs with large drain-gate breakdown voltage are pivotal components for the booming market of wireless and personal communications, since they are required in handset and portable units as well as in base station amplifier circuits. A detailed study of their breakdown behavior is thus extremely urgent and important for the industrial development and exploitation of these devices. In this framework, we give in this abstract an analysis of the gate reverse current under off-state breakdown conditions, which are likely the most critical for the reliability of GaAs-based FETs operated in class AB or B for high-efficiency power amplification. A study of the temperature dependence of the gate reverse current allows us to identify the physical phenomena taking place in the drain-gate region at different values of the reverse bias and to pinpoint the mechanism giving rise to off-state breakdown.

The power HFETs we studied, which represent an attractive compromise for the industrial production of power FETs for X- and Ku-band applications, were fabricated using a double-recess process in production at Alenia. They have 75 nm thick n-GaAs channel, Si-doped at  $4 \times 10^{17} \text{ cm}^{-3}$  and  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$  barrier layer, Si-doped at  $2 \times 10^{17} \text{ cm}^{-3}$ , 30 nm thick under the gate. The T-shaped gate has a length and width of 0.7  $\mu\text{m}$  and 200  $\mu\text{m}$ , respectively. The gate metallization is made of a 0.2  $\mu\text{m}$  Ti layer with 0.45  $\mu\text{m}$  of Al on top. The gate barrier height and ideality factor are 0.81 eV and 1.08, respectively. The devices are passivated by PECVD SiN. Typical devices show  $I_{\text{DSS}} = 300 \text{ mA/mm}$ ,  $V_T = -2.5 \div -3 \text{ V}$ ,  $g_{\text{msat}} = 150 \text{ mS/mm}$ ,  $\text{BV}_{\text{DG}} = 14 \div 16 \text{ V}$  (measured at  $I_G = -1 \text{ mA/mm}$  with source floating). A schematic cross-section is shown in Fig. 1.

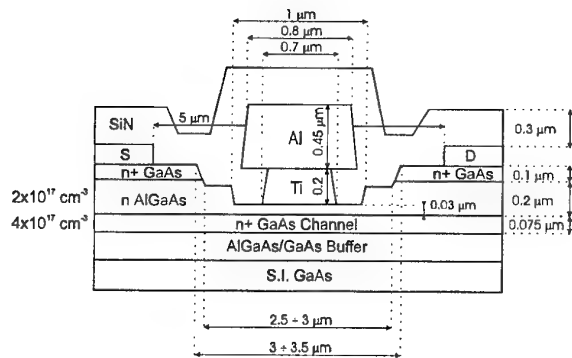
An unambiguous way of defining and measuring the off-state breakdown voltage under three-terminal conditions (which are practically more relevant than the usual two-terminal, floating-source configuration used for breakdown voltage measurement) is that proposed by Bahl and del Alamo [1]. While a fixed  $I_D$  is injected into the device drain (e.g.,  $I_D = 1 \text{ mA/mm}$ ),  $V_{\text{GS}}$  is ramped down from forward bias to pinch-off and the loci of  $V_{\text{DS}}$ ,  $V_{\text{DG}}$  and  $I_G$  are traced as a function of  $V_{\text{GS}}$ . The off-state drain-source breakdown voltage  $\text{BV}_{\text{DS}}$  is then defined as the peak value of the  $V_{\text{DS}}$  locus, while the standard two-terminal drain-gate  $\text{BV}_{\text{DG}}$  is measured where  $I_G = -I_D$ .

We applied this measurement technique to our HFETs at different ambient temperatures ( $T$ ); the  $V_{\text{DS}}$  loci obtained injecting a constant  $I_D = 1 \text{ mA/mm}$  are shown in Fig. 2. The peaks of the  $V_{\text{DS}}$  loci indicate increasing values of  $\text{BV}_{\text{DS}}$  as  $T$  is raised from  $-50^\circ\text{C}$  to  $75^\circ\text{C}$ , as illustrated by Fig. 3. A clear linear dependence exists between  $\text{BV}_{\text{DS}}$  and  $T$  with a positive slope of about  $12 \text{ mV}/^\circ\text{C}$ . This positive slope is a first indication that impact ionization is the origin of the gate reverse current in the pre-breakdown region, since the carrier multiplication rates have a negative temperature coefficient in GaAs [2].

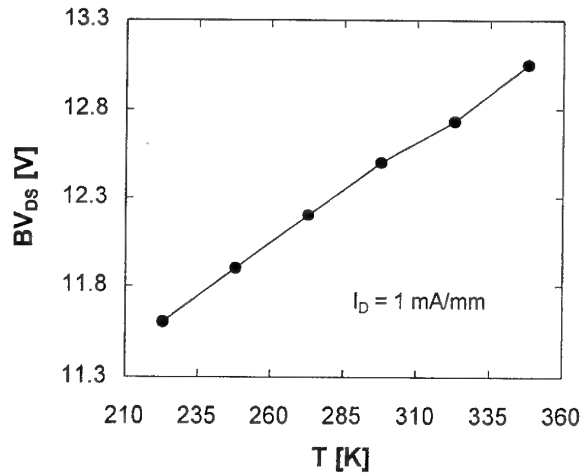
Further evidence of this is given in Fig. 4, where the gate reverse current measured during the sweep of Fig. 2 is plotted as a function of  $1/V_{\text{DG}}$ , down to the point where  $I_G = -1 \text{ mA/mm}$  (i.e., the breakdown conditions). It is known that under impact ionization conditions  $I_G \propto \exp(-A/E)$  [3], where  $A$  is a constant and  $E$  is an effective electric field in the gate-drain region. Since  $E \propto V_{\text{DG}}$ , we get that a linear dependence must be observed between  $I_G$  plotted on a log scale and  $1/V_{\text{DG}}$ . This is indeed what we see in Fig. 4 in the high-field bias range (i.e., for small  $1/V_{\text{DG}}$ ) ushering breakdown. Moreover, the gate reverse current decreases with increasing  $T$  in this region. On the other hand, for lower electric fields (i.e., larger  $1/V_{\text{DG}}$ ), the curves depart from the exponential trend and the  $V_{\text{DG}}$  dependence gets much weaker. In this low-field range, the gate reverse current increases with increasing  $T$ .

We can therefore conclude that: (1) The gate reverse current is limited by thermionic-field-emission (TFE) at low electric field (positive temperature coefficient and weak  $V_{\text{DG}}$  dependence). (2) At larger  $V_{\text{DG}}$  values, impact ionization becomes the dominant component of  $I_G$  (negative temperature coefficient and exponential dependence on  $-1/V_{\text{DG}}$ ) and breakdown is eventually triggered. These results are in contradiction with those of [4], where the off-state breakdown of power GaAs-PHEMTs and InP-HEMTs is proposed to be tunneling-limited.

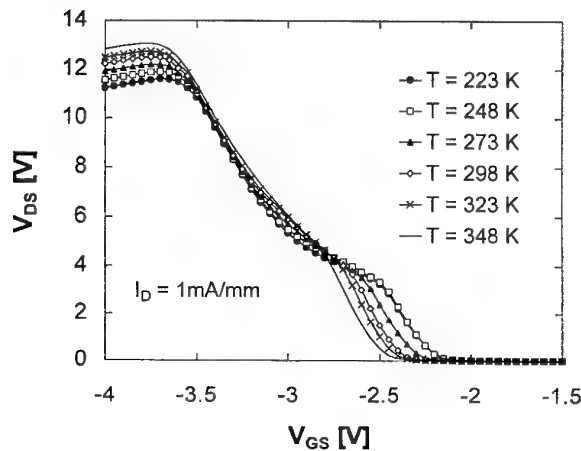
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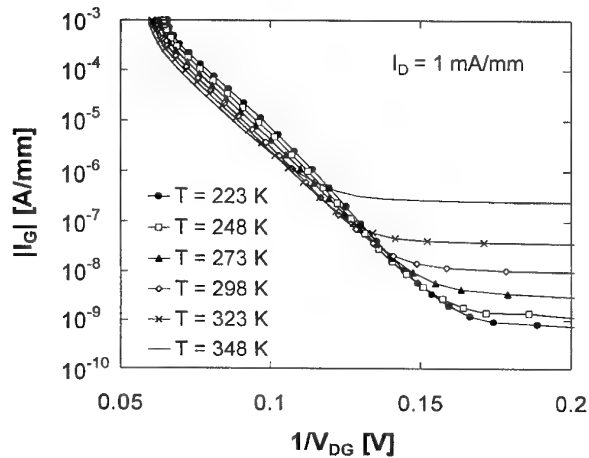
**Fig. 1** Schematic cross-section of the power HFETs under test.



**Fig. 3** Off-state three-terminal drain-source breakdown voltage, as extracted by Fig. 2, versus temperature.



**Fig. 2**  $V_{DS}$  loci obtained injecting a constant  $I_D = 1$  mA/mm and sweeping  $V_{GS}$  from forward bias (not shown) to pinch-off conditions. Each curve corresponds to a different ambient temperature. The off-state three-terminal drain-source breakdown voltage ( $BV_{DS}$ ) is defined as the peak value of each  $V_{DS}$  locus.



**Fig. 4** Gate reverse current magnitude versus  $1/V_{DG}$  at different ambient temperatures, as measured during the sweep of Fig. 2.

# Electroluminescence of composite Channel AlInAs/InGaAs/InP/AlInAs HEMTs

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Impact ionization (I.I.) which induces the generation of electron-hole pairs by avalanche multiplication due to very hot carriers in high electric field regions of semiconductors, is a well-known process in both field-effect and bipolar transistors. It limits in particular the maximum operating voltage of these transistors. This phenomenon is all the more detrimental in InGaAs channel HEMTs on InP since the energy threshold required for ionization is very low due to the small band gap of  $\text{In}_x\text{Ga}_{1-x}\text{As}$  for  $x = 0.53$ . An accurate investigation of impact ionization under different operating conditions is therefore a critical issue. Electrons and holes created by impact ionization can recombine radiatively, giving rise to the so-called electroluminescence (EL). EL spectroscopy constitutes an efficient investigation tool to study impact ionization in HEMTs to probe both the localisation and the energy distribution of carriers versus bias conditions<sup>1</sup>.

In the composite channel InGaAs HEMTs (Fig. 1), an InP layer (sub-channel) is added to the InGaAs channel<sup>2</sup> compared with conventional InGaAs HEMTs. The purpose of this InP layer is that a significant fraction of hot electrons in the InGaAs channel transfer in InP before they reach the threshold of ionisation. Then the electrons which have transferred in InP have a lower kinetic energy. The ionisation rate versus electric field is also weaker in InP because of the wider gap and the large electron effective mass in InP. These different factors contribute to reduce I.I in the transistor<sup>3</sup>.

We present an experimental investigation of impact ionization by electroluminescence in two types of composite channel lattice-matched AlInAs/InGaAs/InP/AlInAs HEMTs with 0.8  $\mu\text{m}$ . The device structure A has an undoped InP sub-channel. The device structure B has a n-doped InP sub-channel ( $1.6 \cdot 10^{18} \text{ cm}^{-3}$ ). The one-state breakdown voltage is 5 V for device A ( $I_{\text{dss}} = 350 \text{ mA/mm}$ ) and 4.5 V for device B ( $I_{\text{dss}} = 560 \text{ mA/mm}$ ). The drain voltage threshold beyond which an EL signal is observable is 2 V for device A and 3.5 V for device B. Fig. 2 shows typical EL spectra measured versus energy at 70 K, in bias conditions corresponding to open channel operation ( $V_{\text{GS}} = 0 \text{ V}$ ,  $V_{\text{DS}} = 3 \text{ V}$  for A and  $V_{\text{DS}} = 5 \text{ V}$  for B). Two main peaks centered respectively near 0.85 eV and 1.23 eV (1.15 eV-1.3 eV) are observed.

The 0.85 eV peak is attributed to direct recombinations in the InGaAs quantum well, of electrons in the first sub-level E1 and of holes in the HH1 sub-level. This assignment is confirmed by numerical simulations which show that, in a 10 nm thick InGaAs well, the E1-HH1 energy difference at 70 K is 0.85 eV. One also observes the recombination between the second sub-level E2 and the sub-level HH1 at 0.93 eV, which is clearly visible as a shoulder at 70 K for device A (Fig. 2a).

The energy value of the peak at 1.23 eV indicates that it is associated with indirect spatial recombinations between electrons in the InP conduction band and holes in the HH1 level of the InAlAs buffer and which are located in the InAs well transition at the interface with InP sub-channel<sup>4</sup>. The observation of the 1.23 eV peak is a direct proof that a fraction of carriers of the InGaAs channel are transferred in the InP sub-channel. But electrons can ionize in InP (in the InAs well transition at the interface with InAlAs). Nevertheless, the sub-channel InP layer reduces impact ionization phenomena and the breakdown voltage in these transistors as compared to standard InGaAs transistors on InP.

We now comment on the integrated intensity variations of the two devices A and B. The main feature is the decrease of the integrated intensity of the 0.85 eV line relatively to the 1.23 eV line for the device B (Fig. 2). Moreover the overall intensity of EL is noticeably reduced. The efficiency of the sub-channel InP layer is better if the InP is n-doped. Indeed the band bending

which results from this n-doping, confines the electrons which are transferred in the InP sub-channel.

We have also investigated the luminescence intensity and the gate current versus biases for both devices A and B. The correlation between the integrated intensity of the 0.85 eV peak and  $I_G$  (Fig. 3), suggests that the holes who reach the gate, are created by II in the InGaAs channel. The gate current of devices A and B for the same  $V_{DS}$  are roughly equal. But the contribution of the electrons to the gate current is more significant for B. Therefore the holes contribution is more significant for A. This observation confirms that the II in the InGaAs is less significant in device B.

|                |        |
|----------------|--------|
| GalAs nid      | 10 nm  |
| $\delta$ -dop  |        |
| AlInAs barrier | 30 nm  |
| GalAs nid      | 10 nm  |
| InP n.i.d      | 25 nm  |
| AlInAs buffer  | 100 nm |
| substrate      |        |

Fig. 1: Layers structure of the composite channel HEMT.

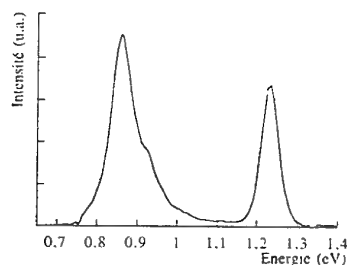


Fig. 2 a): EL spectrum of device A at 70 K for  $V_{DS} = 3$  V and  $V_{GS} = 0$  V.

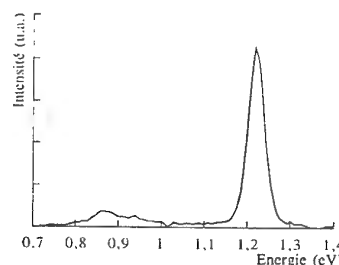


Fig. 2 b): EL spectrum of device B at 70 K for  $V_{DS} = 4.5$  V and  $V_{GS} = 0$  V.

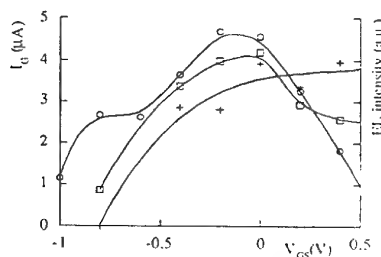


Fig. 3 a): Gate current (square) and integrated EL intensity for device A, of the 1.23 eV line (cross) and the 0.85 eV line (circle) versus gate voltage at 70 K and  $V_{DS} = 3$  V.

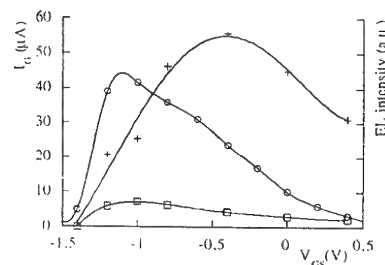


Fig. 3 b): Gate current (square) and integrated EL intensity for device B, of the 1.23 eV line (cross) and the 0.85 eV line (circle) versus gate voltage at 70 K and  $V_{DS} = 4.5$  V.

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## Influence of deep levels in AlInAs/GaInAs/InP HFETs

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### Abstract

AlInAs/InGaAs/InP composite channel HFETs are good candidates for applications in optoelectronic integrated circuits (OEICs). Such devices combine the advantages of high mobility at low voltages and high electric field operations thanks to the use of a composite channel formed by a thin InGaAs layer and a doped InP sub-channel. However, parasitic phenomena are often observed in the characteristics of these transistors. For instance, it is well known that the use of InGaAs channel leads to impact ionization process sometimes responsible of large output conductance variations. Such a phenomenon is intrinsic to the use of InGaAs and can be more or less reduced by using an optimal device architecture, however, extrinsic defects introduced during epitaxial growth or technological steps for device processing can also strongly influence the device performances.

In this work, a detailed study of deep levels in various HFETs structures is presented. These deep levels have been characterized using DLTS, CTS (fig.1), Drain Lag, and low frequency noise (LFN) measurements (fig.2). Electrical characterization of our devices have been also performed under optical excitation (fig.3) in order to study the optical properties of the defects. Indeed, the study of photo-ionization of deep levels gives useful information for a good interpretation of the results obtained by thermal or low frequency excitation techniques.

The main traps observed in our HFETs have been correlated to the AlInAs material in the buffer layers, but also in the barrier layers. Other traps located in the channel/buffer, or in the channel regions have also been detected. Finally, the main deep level which has been identified as E3 in AlInAs is shown to be responsible of a strong generation-recombination noise at room temperature. It is also shown that this trap also contribute to a strong output conductance variation.

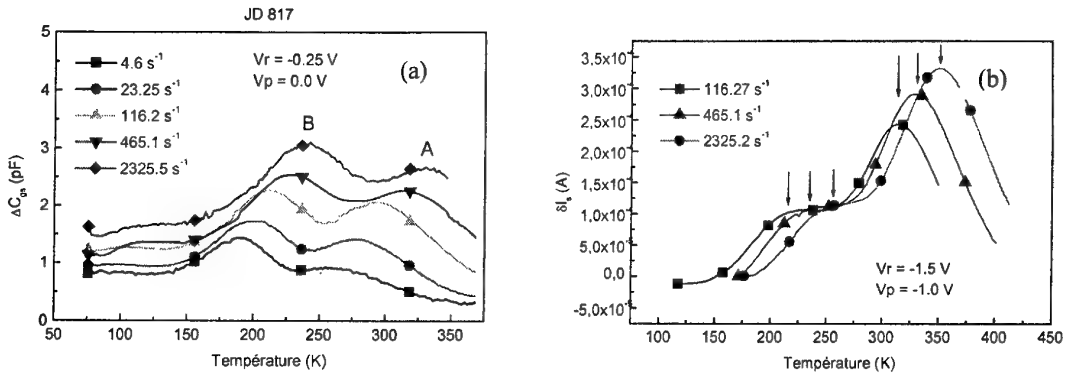


Fig.1 : DLTS spectra of bulk the AlInAs material used in HFET devices (a).  
Current transient spectroscopy spectra recorded for the drain-source currents of the HFETs (b).

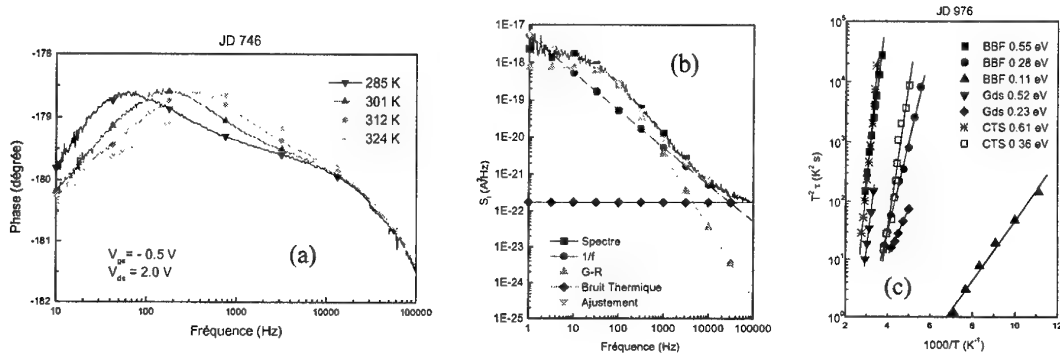


Fig.2 : Phase shift between  $I_{ds}$  and  $V_{ds}$  recorded at various temperatures (a). G-R noise component at 300K in the LFN spectra (b). Trap signatures obtained by three techniques on the same transistor (c).

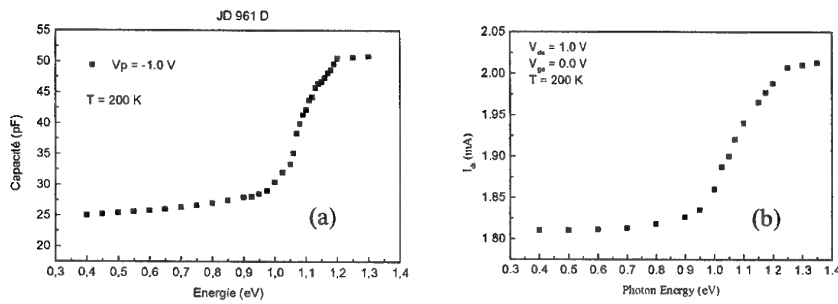


Fig.3 : Variation of the capacitance of a Schottky diode as a function of incident photon energy(a).  
Variation of the drain-source current as a function of incident photon energy(b).

# LOW FREQUENCY NOISE COMPARISON BETWEEN InP/InGaAs AND Si/SiGe HETEROJUNCTION BIPOLAR TRANSISTORS

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## INTRODUCTION

Heterojunction bipolar transistors (HBTs) have shown excellent performances in microwave and lightwave applications. InP/InGaAs and Si/SiGe HBTs are some of the most recent devices. The aim of this study is to compare the excess noise of these two types of transistors. As the knowledge of the  $1/f$  noise level is an important parameter for designers, it is interesting to find out which HBT has the lowest noise level.

## FIRST ORDER MEASUREMENT

From Gummel plots, the base and collector ideality factors  $n_b$  and  $n_c$  have been extracted and are reported in Table 1 for the two types of transistors.

|            | $n_b$ | $n_c$ |
|------------|-------|-------|
| InP/InGaAs | 1.4   | 1.25  |
| Si/SiGe    | 1.1   | 1.06  |

Table 1 : ideality factors for base and collector

First we can remark that for the Si/SiGe HBTs measured values are close to the ideal value of one. Results obtained on InP devices are in good agreement with previous data,  $n_b$  and  $n_c$  are over one, this indicates the presence of a recombination current at the heterointerface.

Two kinds of evolution for the static current gain ( $\beta$ ) can be observed. For the InP HBTs,  $\beta$  increases regularly from 30 to 100 for a collector current density comprised between  $10^3$  A/cm<sup>2</sup> to  $10^5$  A/cm<sup>2</sup>. For the SiGe HBTs,  $\beta$  is nearly constant (65) for  $10^2$  A/cm<sup>2</sup>  $\leq$   $J_c \leq$   $10^4$  A/cm<sup>2</sup>, this constant value being followed by a decrease of  $\beta$ .

## NOISE RESULTS

Noise measurements have been performed in a high impedance common emitter configuration. In order to compare the results the spectral current density referred to the input is calculated:  $S_{i_n} = \frac{S_{v_c}}{(R_L h_{fe})^2}$

(the voltage collector spectral density  $S_{v_c}$  is measured across the bias resistance  $R_L$  and  $h_{fe}$  is the dynamic current gain).

In figure 1 we present a typical behaviour of  $S_{i_n}$  versus frequency for the InP HBTs. We observe that the excess noise is mainly composed of  $1/f$  noise and one g-r component is found around  $10^4$  Hz. The

white noise is never reached in the frequency range used (1 Hz – 100 kHz.).

For the SiGe transistors, two types of spectra have been found. In the first case, presented in figure 2, the  $1/f$  noise is partially masked by several g-r components so its value is not accurately measured. The white noise is reached for low values of the bias current. We have also noted the presence of RTS noise. In the second case (figure 3), the current spectral density is only composed of  $1/f$  noise and the white noise  $2qI_b$  is reached.

Experimentally, the spectral density  $S_{i_n}$  is proportional to  $I_b^{A_f}$ . As shown in figure 4, for the InP HBTs, we measured  $A_f = 1.4$  and for the SiGe HBTs  $A_f = 2$ . This last value, previously found for SiGe [1], is currently observed on polysilicon bipolar transistor [2].

A typical example presented in figure 4, for devices with the same emitter area shows that InP transistors are noisier than SiGe ones.

To analyse  $S_{i_n}$ , the SPICE model is used:

$$S_{i_b} = K_f \frac{I_b^{A_f}}{f^\gamma} \quad (\gamma \approx 1). \text{ The } K_f \text{ coefficients are}$$

extracted and presented in figure 5 versus emitter area. The extracted values are not comparable because the  $K_f$  units are different. For InP  $K_f$  is expressed in (Ampere)<sup>0.6</sup> and for SiGe  $K_f$  is without unit.

## ANALYSIS AND CONCLUSION

For the InP HBTs the evolution of  $S_{i_n}$  with the bias current and  $K_f$  with the geometric characteristics have shown that the noise sources are located in the intrinsic transistor and also at the emitter periphery [3].

Concerning the SiGe HBTs with RTS, the  $K_f$  coefficient is nearly constant. As no notable evolution with the geometric parameters is observed, we can suppose that the noise sources are mostly located in the extrinsic part of the transistor. For the SiGe transistors without RTS only one area is studied, thus the location of the  $1/f$  noise sources is not possible.

The Si/SiGe HBTs studied in this paper are noiseless than the InP/InGaAs ones. But these last transistors

have shown better performances in the high frequency domain. It is also important to underline the interest of the spectrum analyse for circuit designers. Indeed the presence of GR components associated to RTS can significantly increase the  $1/f$  noise level and change its evolution with geometrical parameters. This can have a negative effect for circuits modelling.

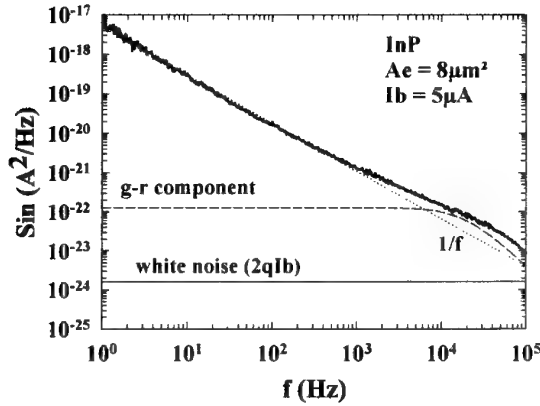


Figure 1 : Typical decomposition of a collector spectral density into several noise components for the InP HBTs.

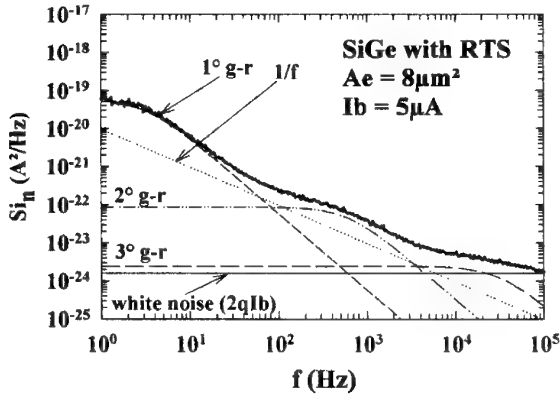


Figure 2 : First example of a decomposition of a collector spectral density into several noise components for a SiGe HBTs.

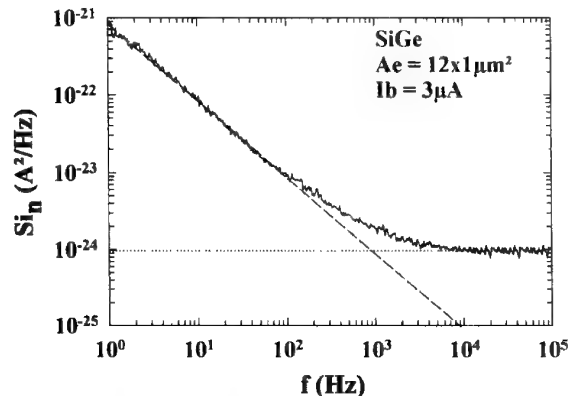


Figure 3 : Second example of a decomposition of a collector spectral density into several noise components for the SiGe HBTs.

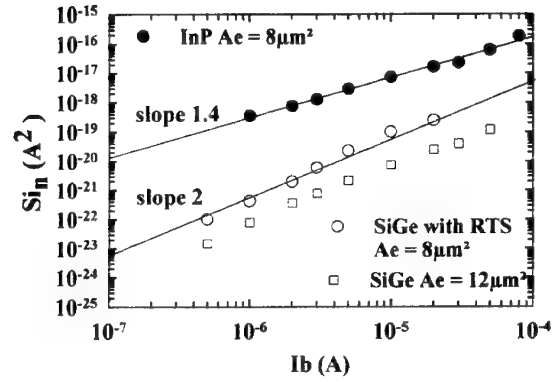


Figure 4 : Values of  $Si_n$  at 1Hz for the two technologies, for different emitter areas.

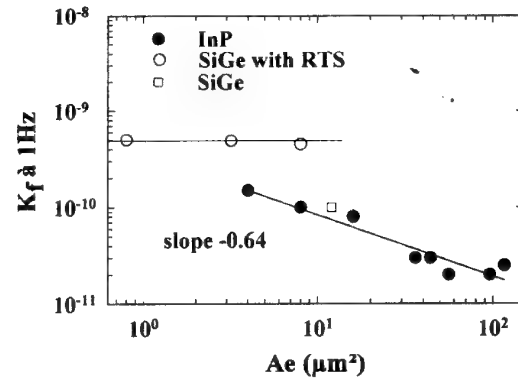


Figure 5 : Values of  $K_f$  at 1Hz for the two technologies versus the emitter area. For InP  $K_f$  is expressed in  $(\text{Ampere})^{0.6}$  and for SiGe  $K_f$  is without unit.

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## Interwell-transfer noise in InP-based InGaAs channels caused by electron tunneling at equilibrium and low electric fields

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Hot electron real-space transfer in modulation-doped heterostructure channels is known to cause negative differential resistivity and other high-field phenomena [1]. In particular, the real-space-transfer noise has been resolved in AlGaAs/GaAs and AlInAs/InGaAs channels at high electric fields applied along the channel [2, 3]. On the other hand, almost no attention has been paid to real-space transfer noise in quantum well channels subjected to low electric fields. In this report we present experimental results obtained for heavily doped InP-based InGaAs quantum well channels and discuss the noise caused by the interwell transfer fluctuations present at equilibrium and low electric fields.

Let us consider an AlInAs/InGaAs/AlInAs quantum-well structure selectively-doped with a thin layer of donors located in AlInAs. Light doping produces no two-dimensional electron gas (2DEG) since all electrons are consumed by the surface states. At moderate doping the Fermi level approaches the bottom of the conduction band in InGaAs, and a high-mobility 2DEG forms in the quasi-rectangular well. Simultaneously, an empty V-shaped quantum well appears in the doped AlInAs barrier layer (Fig. 1). Provided the doping is increased, the upper well becomes deeper, and eventually its occupation starts at certain critical 2DEG density - a low-mobility 2DEG forms in the doped AlInAs.

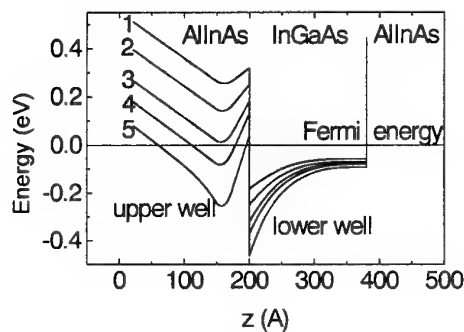


Fig. 1. Effect of doping on quantum well potential in an AlInGa/InGaAs/AlInAs structure containing a thin donor-doped layer AlInAs and no cap layer. Donor density: 1 -  $3.1 \cdot 10^{12} \text{ cm}^{-2}$ , 2 -  $4.1 \cdot 10^{12} \text{ cm}^{-2}$ , 3 -  $5 \cdot 10^{12} \text{ cm}^{-2}$ , 4 -  $6.6 \cdot 10^{12} \text{ cm}^{-2}$ , 5 -  $11.9 \cdot 10^{12} \text{ cm}^{-2}$ . Density of the occupied surface states is  $1.5 \cdot 10^{12} \text{ cm}^{-2}$ .  $T_0 = 80 \text{ K}$ .

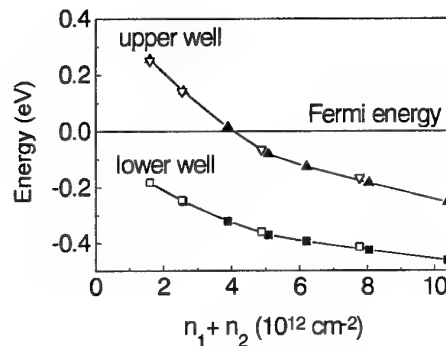


Fig. 2. Dependence of the quantum well bottom energy on the total 2DEG density for two fixed densities of the occupied surface states:  $0.75 \cdot 10^{12} \text{ cm}^{-2}$  (closed symbols) and  $1.5 \cdot 10^{12} \text{ cm}^{-2}$  (open symbols). Triangles stand for the upper well, squares stand for the lower one (see Fig. 1).  $T_0 = 80 \text{ K}$ .

The critical density can be estimated from a self-consistent solution of the coupled Schrödinger-Poisson equations. For a chosen model and a given density of the occupied surface states ( $1.5 \cdot 10^{12} \text{ cm}^{-2}$ ) the critical donor density (where the Fermi level touches the upper well) is around  $5 \cdot 10^{12} \text{ cm}^{-2}$  (Fig. 1). The critical donor density depends on the density of the surface states. Unlike this, the critical 2DEG density is almost independent of density of the occupied surface states (Fig. 2).

The interwell transfer of electrons causes fluctuations of electron densities in the wells and the longitudinal fluctuations of the drift velocity in the direction of the mean current. The spectral density of the resultant velocity fluctuations can be approximated as follows:

$$S_v = S_1 n_1 / (n_1 + n_2) + S_2 n_2 / (n_1 + n_2) + 4 n_1 n_2 / (n_1 + n_2) (v_1 - v_2)^2 \tau, \quad (1)$$

where  $v_i$ ,  $S_i$ , and  $n_i$  are the drift velocity, the spectral density of velocity fluctuations, and the 2DEG density in the  $i$ -th well,  $\tau$  is the time constant of the interwell transfer. The last term in Eq. (1) stands for the interwell transfer contribution. It increases proportionally to the squared electric field ( $E^2$ -dependence) at low electric fields where the Ohm's law holds. Since  $\mu_i$ ,  $n_i$ , and  $\tau$  are field-dependent, some deviations from the  $E^2$ -dependence develop at higher electric fields. At high fields, the drift velocities,  $v_1$  and  $v_2$ , tend to saturate, and their difference tends to zero - the interwell transfer contribution tends to decrease.

The expected behaviour is observed experimentally in heavily doped AlInAs/InGaAs/AlInAs heterostructures (Fig. 3). The data at different temperatures show (Figs. 3 (a) and (b)), that the interwell transfer contribution increases upon cooling: there is no thermal activation. This supports the idea of a non-activated electron tunneling responsible for the interwell transfer present at thermal equilibrium and low electric fields.

Unlike this, the fields exceeding 2 kV/cm are required for the onset of hot electron real-space-transfer noise in moderately doped channels containing no low-mobility 2DEG channel at thermal equilibrium [3].

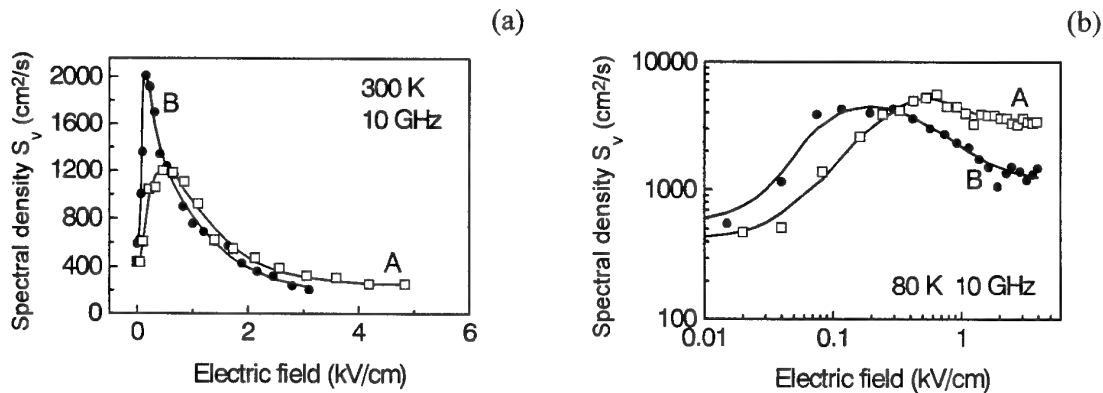


Fig.3. Longitudinal spectral density of velocity fluctuations in InP-based lattice-matched InAlAs/InGaAs/InAlAs heterostructures at: (a) 300 K and (b) 80 K. Electron mobility and 2DEG density: A -  $\mu_{300} = 4200 \text{ cm}^2/\text{Vs}$ ,  $\mu_{80} = 15200 \text{ cm}^2/\text{Vs}$ ,  $n_{300} = 8.6 \cdot 10^{12} \text{ cm}^{-2}$ ,  $n_{80} = 7.6 \cdot 10^{12} \text{ cm}^{-2}$ ; B -  $\mu_{300} = 5700 \text{ cm}^2/\text{Vs}$ ,  $\mu_{80} = 19900 \text{ cm}^2/\text{Vs}$ ,  $n_{300} = 6.3 \cdot 10^{12} \text{ cm}^{-2}$ ,  $n_{80} = 5.3 \cdot 10^{12} \text{ cm}^{-2}$ .

### Acknowledgements

The authors thank Prof. E. Kohn and Dr. B. Henle with Ulm University for the MBE-grown heterostructures.

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Wednesday, May 26, 1999 16:25

## Technology

- *Doping profile extraction method with the sub-Debye length resolution*  
M.F. Kokorev, N.A. Maleev<sup>(1)</sup>, and A.G. Kuzmenkov  
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p. 59
- *Very high selective wet etching : application to the uniformity improvement of linear power PHEMT*  
X. Hue, B. Boudart, B. Bonte, and Y. Crosnier  
University of Lille-IEMN, Villeneuve d'Ascq, France

p. 61
- *Small-size ohmic contacts to A3B5 semiconductor devices*  
T.A. Briantseva, D.V. Lioubchenko, and V.E. Lyubchenko  
Institute of Radioengineering and Electronics, Moscow, Russia

p. 63
- *Indium tin oxide spreading layers for high performance visible LED's*  
D.V. Morgan, I.M. Al-Ofi, and Y.H. Aliyu  
Cardiff University, Cardiff, UK

p. 65
- *The present state of production and development of III-V compounds in Elma-Malachit*  
A. Arendarenko and Yu Sveshinikov  
JSC Elma-Malachit, Moscow, Russia

p. 67

# DOPING PROFILE EXTRACTION METHOD WITH THE SUB-DEBYE LENGTH RESOLUTION

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It is well known that classical C-V profiling is inapplicable for the structures where the doping profile considerable changes on the distances below the Debye length  $\lambda_D$ . However, up to now the C-V profiling is a major method of non-destructive doping profile characterization for micro- and nanostructures [1]. To raise the spatial resolution of C-V profiling the concept of inverse modeling has been proposed [2].

In this work, we report on the efficient doping profile extraction method with the sub-Debye length resolution based on the concept of inverse modeling.

The classical C-V profiling procedure is described by the following expressions:

$$N_{ap}(W) = -C(V)^3 / (e\epsilon dC / dV), \quad W = \epsilon / C(V), \quad (1)$$

where  $N_{ap}$  is the C-V (or apparent) profile,  $W$  is the depth of the depletion layer,  $C$  is the capacitance per unit area,  $V$  is the reverse bias applied to a Schottky barrier placed in space coordinate point  $z=0$ ,  $e$  is the electron charge, and  $\epsilon$  the permittivity of the semiconductor. In Eq.(1) space coordinate set  $W$  can be treated as the image of initial voltage coordinate set  $V$ . However, the computer simulation demonstrates that the thermal motion of electrons moves the point  $W$  respect to the true edge of the depletion layer  $W_d$ . So, the space coordinate set  $W_d$  must be equivalent to the initial voltage coordinate set  $V$ . The transformation of coordinates gives the relationship between apparent profile and extracted doping profile:

$$N_{ext}(W_d) = (dW / dW_d) N_{ap}(W_d), \quad (2)$$

where  $N_{ext}(W_d)$  is the extracted doping profile,  $W=W(W_d)$ ,  $dW/dW_d$  is the Jacobian, and  $N_{ap}(W_d)$  is the apparent profile in coordinates  $W_d$ . In such approach the coordinate  $W$  can be called *apparent* and coordinate  $W_d$  can be considered as *true*.

The true coordinate  $W_d$  can result from numerical calculation of *the distribution function for the perturbed space charge density*  $\rho(z, V)$  (or  $\rho$ -function) normalized by following condition:

$$\int_0^L \rho(z, V) dz = 1, \quad (3)$$

where  $L$  is the total length of the structure [3]. This function describes the spatial localization of charge density stimulated by small-signal voltage perturbation. The first absolute moment  $\langle z \rangle$  gives  $W(V)$  :

$$W(V) = \langle z \rangle = \int_0^L z \rho(z, V) dz. \quad (4)$$

It is very important that the shape of  $\rho$ -function is unimodal and depends only on the doping profile  $N_d(z)$ . In general, the mode  $W_m$  (i.e. the maximum position) does not coincide with  $W$ . For the uniform doping profile the displacement  $W - W_m$  is constant and  $dW/dW_m = 1$ . However its changes in the non-uniform regions. That is why we assume

$$W_d = W_m. \quad (5)$$

The proposed doping profile extraction method includes: 1. Determination of the apparent profile using Eq.(1); 2. Iterative procedure involving the numerical solution of the nonlinear Boltzmann-Poisson equation for given voltages  $V$ , the numerical solution of the linear equation for the  $\rho$ -function (forward modeling) [3] and Eq.(2) (inverse modeling).

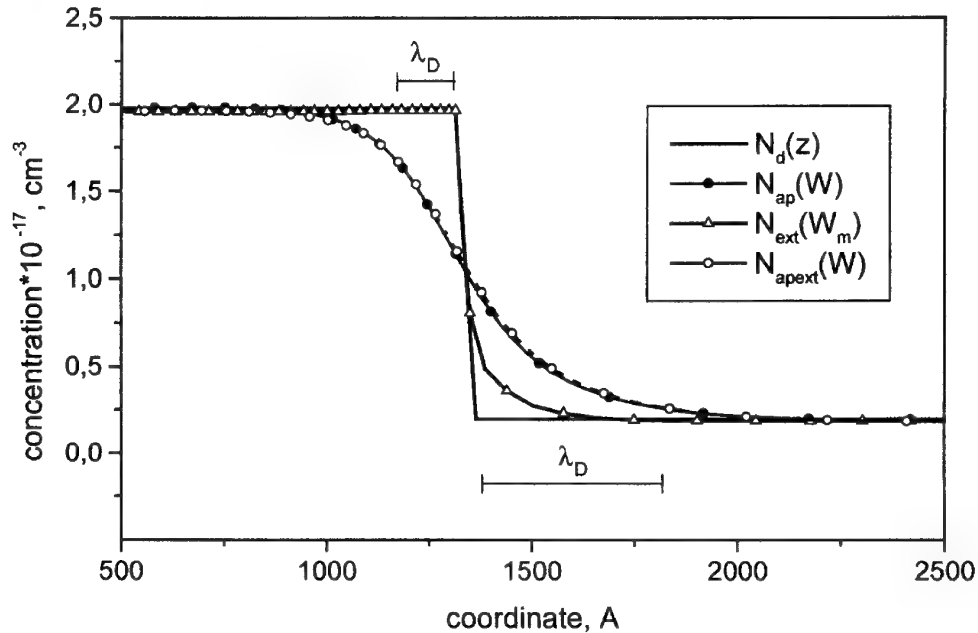


Fig.1. Doping profile extraction for GaAs  $n^+n$  structure.

Fig.1 illustrates the doping profile extraction results for GaAs  $n^+n$  structure. The initial apparent profile  $N_{ap}(W)$  was numerically simulated for given doping profile  $N_d(z)$ . The apparent profile  $N_{apext}(W)$  corresponds to the extracted profile  $N_{ext}(W_m)$ . It is clear that the proposed doping profile extraction method has the sub-Debye length resolution.

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## Very high selective wet etching: application to the uniformity improvement of linear power PHEMT

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Linear solid state power amplifiers are required for applications like telemetry or multimedia telecommunications in Ku band. In order to limit third order intermodulation distortion generated by power amplifiers, it is necessary to reduce the device non-linearities. GaAs material is a good candidate for space applications due to its low radiation sensitivity and good thermal dissipation. Moreover the AlGaAs/InGaAs PHEMT has demonstrated its capability to deliver a high power density of 1 W/mm at 30 GHz [1].

From this generic structure, a PHEMT with two channels (the upper in GaAs and the other in InGaAs material), has been optimized to obtain high linearity and high power simultaneously. For power applications, multifinger structures with large gate developments are necessary. But in that case, high electrical characteristic uniformity is expected to minimize the non-linearities due to technological aspects.

To improve the electrical characteristics uniformity, we have used a citric acid / hydrogen peroxide / ammonium hydroxide solution [2] to selectively etch the gate recessing of AlGaAs/InGaAs/GaAs multifingers PHEMTs. Moreover, the gate recess control permits to obtain a high breakdown voltage value and to keep a high drain current value.

The PHEMT structure used in this study was grown by solid source molecular beam epitaxy. It consisted of a 70 nm  $n^+$  GaAs cap layer with a doping level of  $5 \times 10^{18} \text{ cm}^{-3}$ , a 20 nm undoped  $\text{Al}_{0.22}\text{Ga}_{0.78}\text{As}$  Schottky barrier, a first Si  $\delta$ -doping ( $3.5 \times 10^{12} \text{ cm}^{-2}$ ) with an undoped GaAs channel followed by a second Si  $\delta$ -doping ( $3.5 \times 10^{12} \text{ cm}^{-2}$ ) with an undoped  $\text{In}_{0.22}\text{Ga}_{0.78}\text{As}$  channel (figure 1).

The process fabrication started with device isolation through mesa etching. The Ni/Ge/Au/Ti/Au ohmic contacts were annealed at 400°C during 40 s. Ti/Pt/Au was evaporated for the gate metallization. The gate length was 0.2  $\mu\text{m}$ . The source drain distance was 1.3  $\mu\text{m}$ . The total gate width increases from 2x20 $\mu\text{m}$  to 8x75 $\mu\text{m}$  and needs airbridges realization to ground the sources. A  $\text{Si}_3\text{N}_4$  film was deposited in a plasma enhanced chemical vapor deposition reactor to passivate the device and to minimize the effects of electrical stress on the gate breakdown voltage [3].

The I-V characteristics at room temperature of a 8x50x0.2  $\mu\text{m}^2$  PHEMT is presented in Figure 2. The maximum drain current value is 700 mA/mm at  $V_{gs} = +0.8 \text{ V}$ . It clearly presents a linear variation versus the gate source voltage. The breakdown voltage in diode configuration is -10V, at 1 mA/mm gate current.

Figure 3 shows the drain current density histogram for  $V_{gs} = +0.8 \text{ V}$  measured across the sample and realized over more than 100 components with different gate widths. Very good standard deviation values of 39 mA/mm and 32 mV have been respectively obtained for the drain current and the threshold voltage.

RF characterization indicates high gain value ( $\text{MAG} = 12 \text{ dB}$  at 25 GHz) over a large gate voltage swing. As we can see in figure 4, the IP3 value, measured at 16GHz for a  $V_{ds}$  of 3V and for a 2x75x0.2 $\mu\text{m}^2$  gate development, is 25dBm.

Acknowledgment :

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|  |        |
|--|--------|
| GaAs 5x10 <sup>18</sup> cm <sup>-3</sup> | 70 nm  |
| Al <sub>0.22</sub> Ga <sub>0.78</sub> As | 20 nm  |
| GaAs                                     | 0.4 nm |
| δSi                                      |        |
| GaAs                                     | 0.4 nm |
| Al <sub>0.22</sub> Ga <sub>0.78</sub> As | 3 nm   |
| GaAs                                     | 12 nm  |
| AlAs/GaAs 6x                             | 5 nm   |
| δSi                                      |        |
| GaAs                                     | 0.4 nm |
| Al <sub>0.22</sub> Ga <sub>0.78</sub> As | 2 nm   |
| GaAs                                     | 1 nm   |
| In <sub>0.22</sub> Ga <sub>0.78</sub> As | 12 nm  |
| GaAs                                     | 1.5 nm |
| Al <sub>0.22</sub> Ga <sub>0.78</sub> As | 150 nm |
| GaAs                                     | 300 nm |
| AlAs                                     |        |
| GaAs substrate                           |        |

Figure 1:

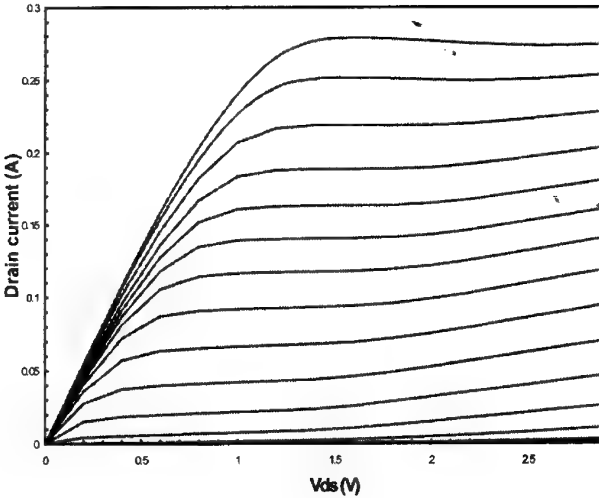


Figure 2: Vgs max=0.8V  
(Vgs step 200 mV)

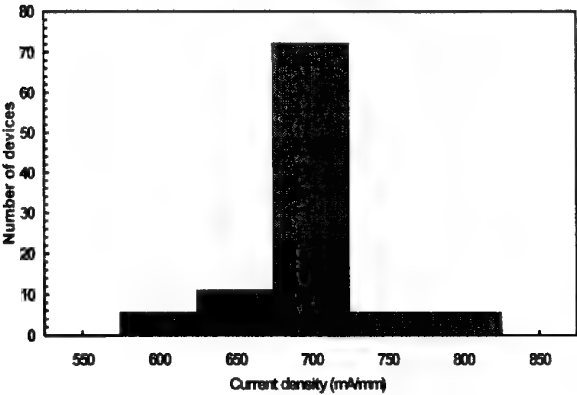


Figure 3

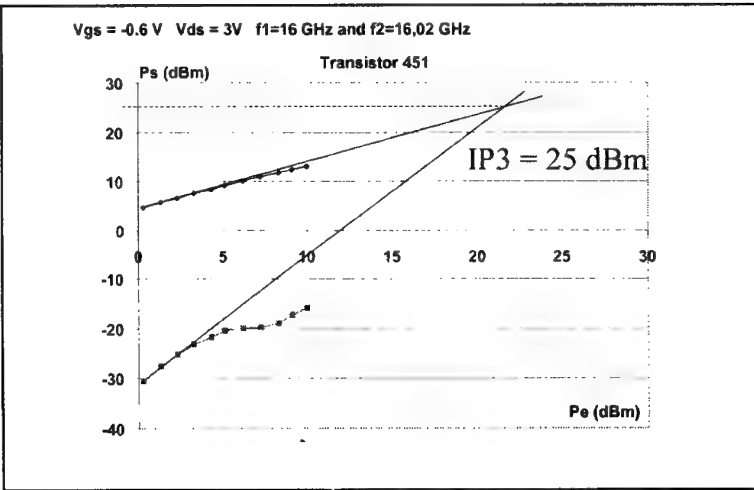


Figure 4:

## Small-size ohmic contacts to A3B5 semiconductor devices

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Small-size Au based ohmic contacts, necessary to Gunn diodes, resonance tunnelling diodes, and other devices, in which operation current density exceeds  $10^4$  A/cm<sup>2</sup> can be performed as honey-comb structures inside the windows, opened in SiO<sub>2</sub> covering layers [1]. The behaviour of Au films on the surface of Au/SiO<sub>2</sub>+GaAs (windows) depends on SiO<sub>2</sub> and Au film thickness as well as on their ratio [2]. This is due to various strains (compressive and expansion) and specific distribution of the strained zones, that appear on the SiO<sub>2</sub>+GaAs (windows) substrate surface during annealing. The strain created in Au layer, in turn, results in defect creation or elimination. It depends on two contrary processes: i) Au atom migration from Au layer on SiO<sub>2</sub> surface to GaAs windows at the temperatures below 450 °C; ii) Ga atom migration from GaAs windows to Au on SiO<sub>2</sub> at temperatures beyond 450 °C. Therefore in the design of honey-comb structures (window sizes, distance between windows, SiO<sub>2</sub> and Au layer thickness and their ratios) these processes should be taken into account. In this work the morphologies and compositions of films were studied by SEM, AES, HEED and precise chemical analysis [3].

Au films when they are thin ( $\sim 0.05$   $\mu\text{m}$ ) appear to be sensitive to microstresses on the SiO<sub>2</sub>+GaAs (windows) and can decorate the effects, caused by distinction of thermal coefficients of GaAs, SiO<sub>2</sub> and Au layers. At the same time thicker Au film ( $\sim 0.4$   $\mu\text{m}$ ) is sensitive to the integrated strains of the whole honey-comb structure and decorates them.

Thin SiO<sub>2</sub> film ( $\leq 0.2 \div 0.3$   $\mu\text{m}$ ) is expanding in accordance with GaAs under thermal treatment, resulting the strains in contrary to this expanding. Au film even at 0.4  $\mu\text{m}$  thickness is sensitive to this strain moving to the centre of sample surface. More thick ( $0.5 \div 0.6$   $\mu\text{m}$ ) oxide layer resists GaAs

expansion and its surface does not have remarkable strains. Au layer remains to be quite homogeneous.

Thin Au film (0.05  $\mu\text{m}$ ) at annealing up to 450  $^{\circ}\text{C}$  has a tendency to occupy the GaAs windows, as most expanding part of  $\text{SiO}_2$ +GaAs (windows) substrate. However with increasing of annealing temperature beyond 450  $^{\circ}\text{C}$  for thin  $\text{SiO}_2$  layers the reversal effect is observed – pulling Au back from window edges to the centre of  $\text{SiO}_2$  cell between windows.

In the case when Au goes for the window centre the defects – pores near window edge are formed and the labyrinth structure appears ( $\text{SiO}_2 \sim 0.5 \mu\text{m}$ ), whereas at  $\text{SiO}_2$  thickness  $\sim 0.2\div 0.3 \mu\text{m}$  the coalescence starts by “hillock” diffusion. In the first case Ga migration to Au film on  $\text{SiO}_2$  is according to slow diffusion mechanism (bulk), in the second case – according to fast diffusion mechanism (grain boundary). Some of these processes were studied before [2].

The results obtained for Au/ $\text{SiO}_2$ +InP (windows) are similar, although the specific parameters are different of Au/ $\text{SiO}_2$ +GaAs system. In both cases low resistance contacts as small as 2  $\mu\text{m}$  in diameter were performed.

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# Indium Tin Oxide Spreading Layers for High Performance Visible LED's

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In this paper, the effectiveness of indium tin oxide (ITO) is evaluated as a current spreading layer for AlGaInP visible light emitting diodes. A range of test device structures has been fabricated to test the current spreading characteristics. The basic test structures are shown in figure 1. These include special devices using GaP spreading layer on which ITO can be compared.

The paper will describe the optical performance of the basic test structure (figure 2) along with the data for a range of devices with increasing chip dimensions. From this study critical parameters in the structure which need to be optimised are identified.

From these results the following conclusions may be drawn. GaP is an effective spreading layer and the 5  $\mu\text{m}$  GaP layer produced the best results to date. However, it needs to be noted that this is a relatively thick layer and reducing the GaP to 1  $\mu\text{m}$  showed it to be relatively ineffective. By comparison, ITO layers of 70 nm have proved to be almost as effective as the much thicker (i.e. 5000 nm) GaP. Its effectiveness as a spreading layer is therefore two orders of magnitude better and would certainly have outperformed GaP in terms of total light output were it not for the facts that at 70 nm it has a finite absorption of around 13% and that the need for a thin GaAs layer to protect the AlGaInP and to form the ohmic contact further increases the near surface absorption.

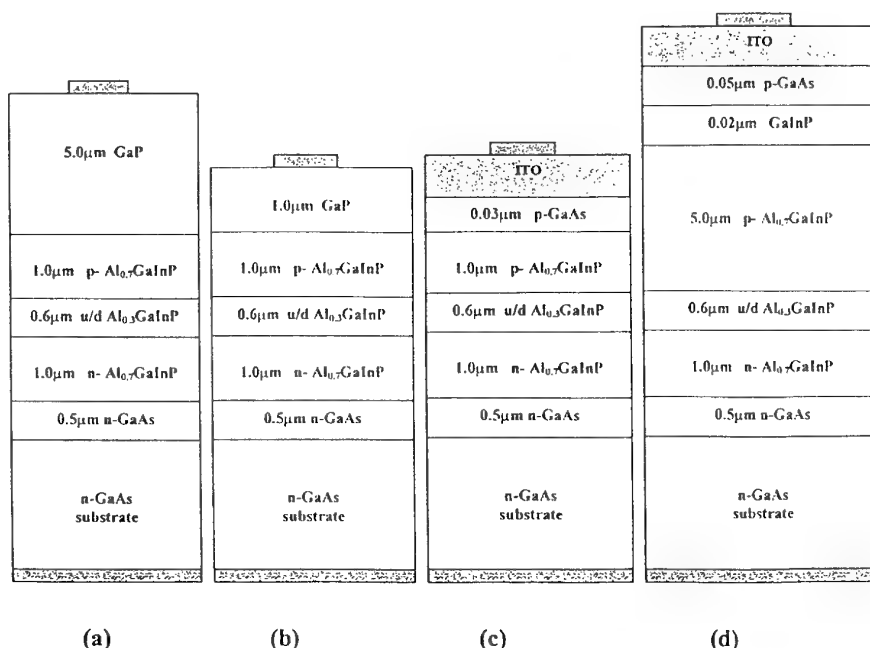


Figure (1): The devices structures; (a), (b) consist of a p-type GaP layer 5  $\mu\text{m}$  and 1  $\mu\text{m}$  respectively, and (c) has no effective spreading layer whilst (d) has an identical active layer with a thicker p-type AlGaInP (5  $\mu\text{m}$ ) and a highly doped GaInP spreading layer. (Not to scale)

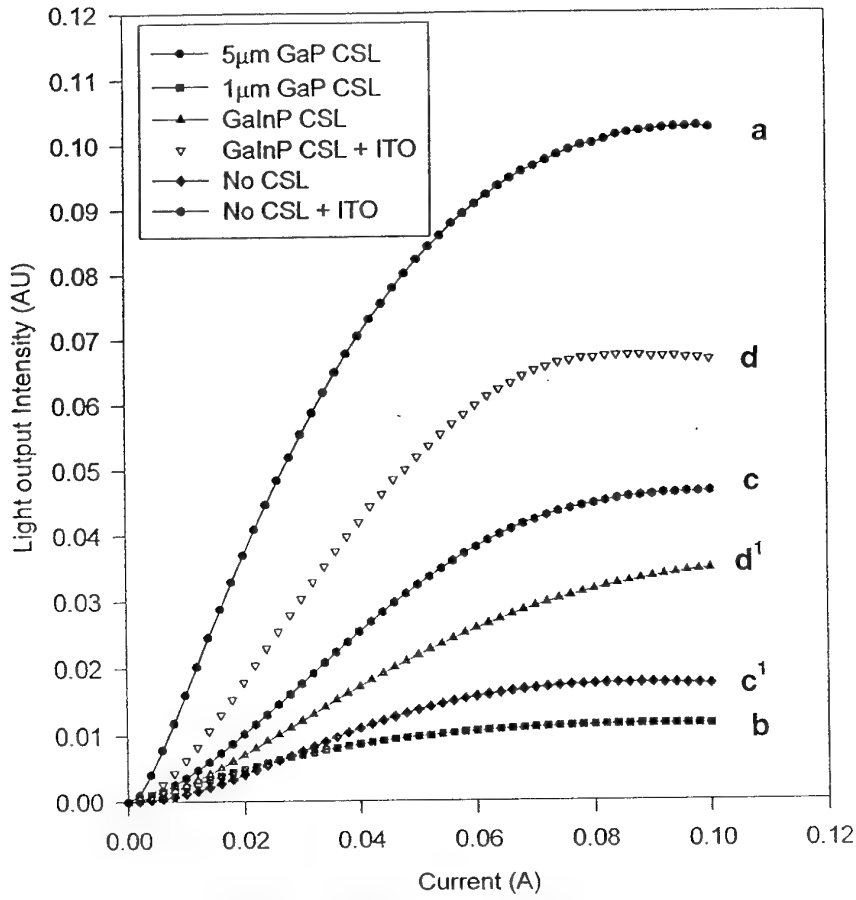


Figure (2): Light output versus input current for different device structures with (500μm×500μm) chip area as shown in Fig. (1).

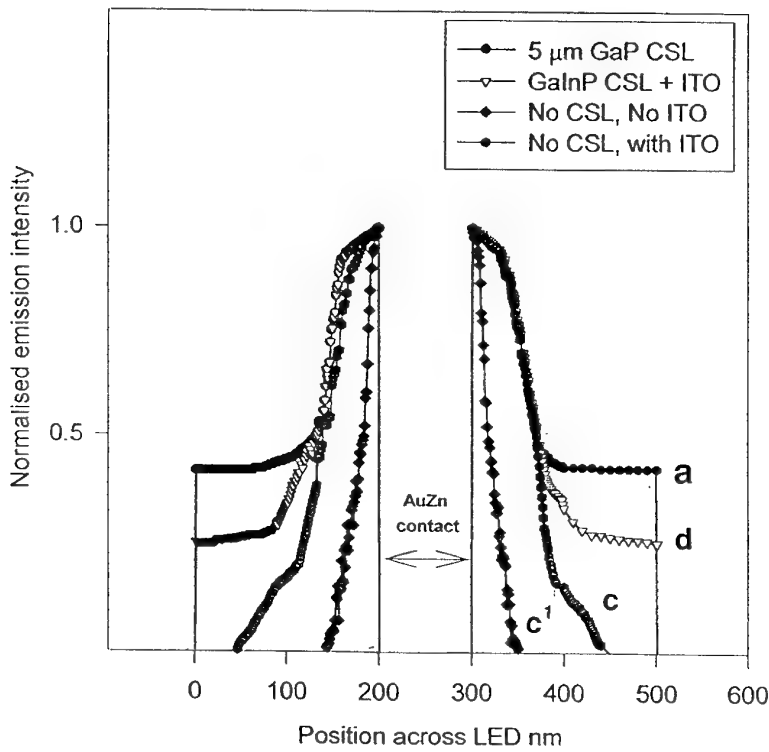


Figure (3): Surface light-emission intensity profiles of different LED chips.

# THE PRESENT STATE OF PRODUCTION AND DEVELOPMENT OF III-V COMPOUNDS IN ELMA-MALACHIT

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JSC ELMA-MALACHIT is a subsidiary enterprise of ELMA association which is one of the largest producers of semiconductor and other materials for electronic industry in Russia. The main line of enterprise activity is production and development of III-V semiconductors: single crystals, slices, epitaxial wafers for various applications.

Single crystals. The main features of producing single crystals are shown in the table.

| Material | Diameter, mm | Dislocation density, $\text{cm}^{-2}$ | Type of conductivity (doping element)           | Growth method |
|----------|--------------|---------------------------------------|---|---------------|
| GaP      | up to 76     | $< 5 \cdot 10^4$                      | n(Si, S),<br>non-doped opto grade               | LEC           |
| GaAs     | up to 76     | $< 1 \cdot 10^4$                      | n(Si, Te), p(Zn),<br>SI (non-doped), opto grade | LEC           |
| InP      | up to 60     | $< 1 \cdot 10^3$                      | n(S), p(Zn), SI (Fe),<br>non-doped              | LEC           |

Production of single crystals 100 and 150 mm in diameter is in preparation. To grow crystals with lowered dislocation density and improved homogeneity of parameters the modified LEC method is under investigation

Slices. ELMA-MALACHIT manufactures a wide range of III-V semiconductor slices using single crystals of own production as well as those from other producers. The main features of wafers meet SEMI standards.

Epitaxial wafers. Various methods of epitaxy (MOCVD, VPE, and LPE) are used for epitaxial wafers growing. The main applications of these materials are optoelectronics, microwave electronics and metrology (Hall sensors, X-ray sensors and so on). MOCVD method is widely used for large-scale production of GaAs epitaxial wafers for FET, mixers, multipliers and other devices and MMICs. Much attention is given to development and manufacture of various heterojunction structures for devices and MMICs of mw technics (HEMT, HBT), as well for optoelectronics (LEDs on the base of AlInGaP, photocathodes).

VPE methods are traditionally used for producing GaAs and GaP wafers with rather thick epitaxial layers. The ability of growing layers up to 100  $\mu\text{m}$  in thickness with controlled carrier concentration level within the range from  $10^{12}$  to  $10^{18} \text{ cm}^{-3}$  enables us to make structures for mw devices (Gann diodes, IMPATT diodes and so on), LED (GaP, GaAsP) as well as for X-ray sensors

LPE method being used mainly for producing GaP structures for green LEDs, also has their own part in total production yield.

We are going also to explore MOCVD epitaxial growth process of nitride compounds for both short wave LEDs and superpower field transistors.

In collaboration with RAN institutes we are involved in the investigation of a new approach to the fabrication of nano-scale structures based on controlled formation of composition ordered epitaxial layers of III-V alloys during MOCVD.

**Wednesday, May 26, 1999 17:40**

# MMIC

- *GaAs MHEMT: The evolution of GaAs-based FETs for high performance microwave and millimeter wave low noise applications (invited paper)* p. 71  
 Thomas Kazior  
 Raytheon Microelectronics, Andover, MA USA
- *A 94 GHz CPW low noise amplifier on InP* p. 75  
 V. Hoel, S. Boret, B. Grimbert, G. Apercé<sup>(1)</sup>, T. Decaesteke<sup>(1)</sup>, S. Bollaert, X. Wallart, S. Lepilliet, and A. Cappy  
 University of Lille-IEMN, Villeneuve d'Ascq, France  
<sup>(1)</sup> Thomson-Detexis, St Cloud, France
- *High-efficiency MMIC power amplifiers using AlGaAs p-HEMT technology* p. 77  
 D. Roques, J-C. Sarkissian, B. Cogo, M. Soulard, J-L. Cazaux, J. Malin<sup>(1)</sup>, D. Shaw<sup>(1)</sup>, and D. Simpson<sup>(1)</sup>  
 Alcatel Space Industries, Toulouse, France  
<sup>(1)</sup> Tri-Quint Semiconductor Texas, USA
- *GaAs PHEMT spice model for very high bit rate digital circuits.* p. 79  
 D. Demange and R. Leblanc  
 Philips Microwave Limeil, Limeil Brevannes, France
- *Composite channel InP HEMT for high cut-off frequency x breakdown voltage performance* p. 81  
 C. Ladner, J. Décobert, S. Sainson, S. Biblemont, G. Post, M. François<sup>(1)</sup>, M. Muller<sup>(1)</sup>  
 OPTO+/CNET, Marcoussis, France  
<sup>(1)</sup> University of Lille-IEMN, Villeneuve d'Ascq, France
- *Characterization of residual carbon in semi-insulating GaAs substrates for integrated circuits* p. 83  
 K.D. Glinchuk, N.M. Litovchenko, A.V. Prokhorovitch, and O.N. Strilchuk  
 Institute of Semiconductors Physics, Kyiv, Ukraine

## **GaAs MHEMT: The Evolution of GaAs-based FETs for High Performance Microwave and Millimeter Wave Low Noise Applications**

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### **Abstract**

State of the art microwave and millimeter wave noise performance and linearity has been demonstrated using GaAs Metamorphic HEMT (MHEMT) technology. The low noise, high gain, excellent linearity and low DC power consumption of the MHEMT coupled with the manufacturability of GaAs make the MHEMT an excellent candidate for cost sensitive, high performance applications. At Raytheon, MHEMT LNAs are currently being designed and fabricated for a wide variety of microwave and millimeter wave applications. The MHEMT is the next step in the evolution of GaAs low noise FET technology.

### **Introduction**

The exploding wireless communications industry has created a rapidly expanding market for microwave devices. While current technology can meet today's needs, advances in microwave device technology are needed in order to realize the wireless (satellite) communications systems of tomorrow. System sensitivity requirements necessitate receivers that operate with lower noise and lower intermodulation distortion (higher linearity). Size, weight and battery lifetime constraints require receivers to operate with extremely low power consumption. Large voice, video and data bandwidths, coupled with the fact that the microwave communication frequency allocation is becoming oversubscribed, require receivers that operate at higher and higher frequencies driving the shift in emphasis from microwave to millimeter wave.

### **Discussion**

The ability to meet future systems requirements hinges upon the performance of the basic building block - the microwave transistor. To date GaAs FET technology has been used to realize LNAs for numerous microwave and millimeter wave applications. Over time the GaAs low noise FET technology has evolved from ion implanted and epitaxial MESFETs to HEMTs and pHEMTs with concomitant improvements in noise performance (noise figure and associated gain). An example of currently available production GaAs pHEMT LNA technology is shown in Figure 1. This 4 stage LNA exhibits 2.6 dB noise figure and 26-28 dB associated gain over a 27 - 31 GHz band while consuming 135 mW of DC power. While this respectable performance is adequate for many of today's systems, it does not meet the requirements of next generation communication systems.

InP-based HEMTs offer a distinct performance advantage over GaAs pHEMT technology, due to the superior transport properties of the high In content InGaAs channel. This performance advantage, however, comes at considerable expense. In addition to the relatively high cost associated with manufacturing InP based devices. InP HEMTs suffer from relatively low on- and off- state breakdown voltages which places restrictions on the operating bias and robustness of these devices.

An attractive, low cost alternative is to fabricate devices with high In content InGaAs channels on GaAs substrates - i.e., the GaAs Metamorphic HEMT (MHEMT) technology [1-4]. This approach is illustrated in Figure 2 - a schematic cross section comparing GaAs pHEMT with 20% In channel, lattice matched InP HEMT with 53% In channel and GaAs MHEMTs with 53 and 35% In channels. In the Raytheon approach, the high In content channel is grown on top of a strain relaxed graded InAlGaAs buffer layer [5]. The unique feature of the MHEMT approach is that the buffer layer can be graded to any In content allowing an

additional degree of freedom in device optimization. Table 1 summarizes the transport properties achieved to date for different MHEMT structures (different channel In content). As can be seen in Table 1, the transport properties of the MHEMT with a 60% In channel are identical to those of a InP HEMT with a 60% In channel indicating the excellent quality of the MHEMT material.

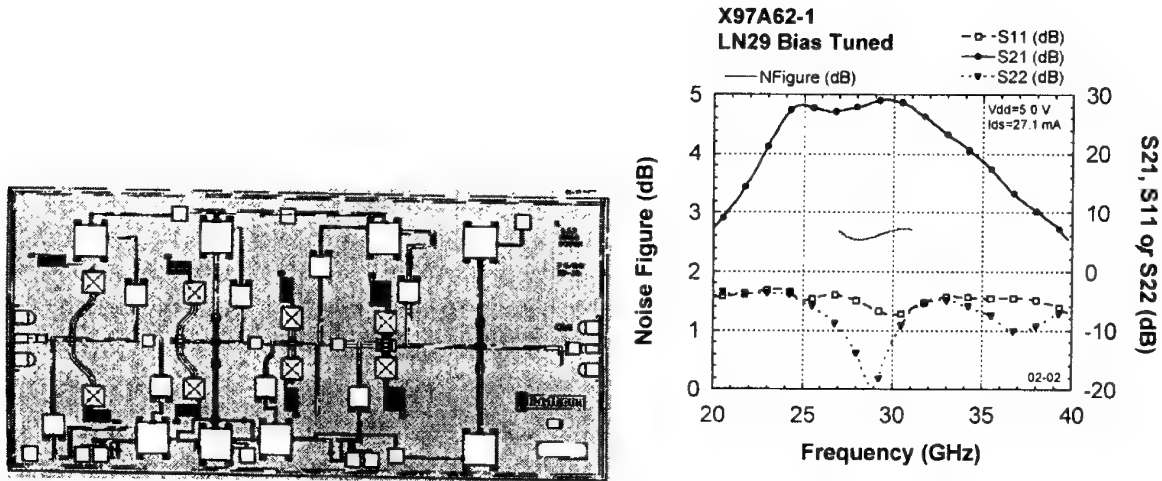


Figure 1: Plot (right) of  $F_{min}$  and Associated Gain versus frequency for a production 4 stage GaAs pHEMT millimeter wave LNA (left).

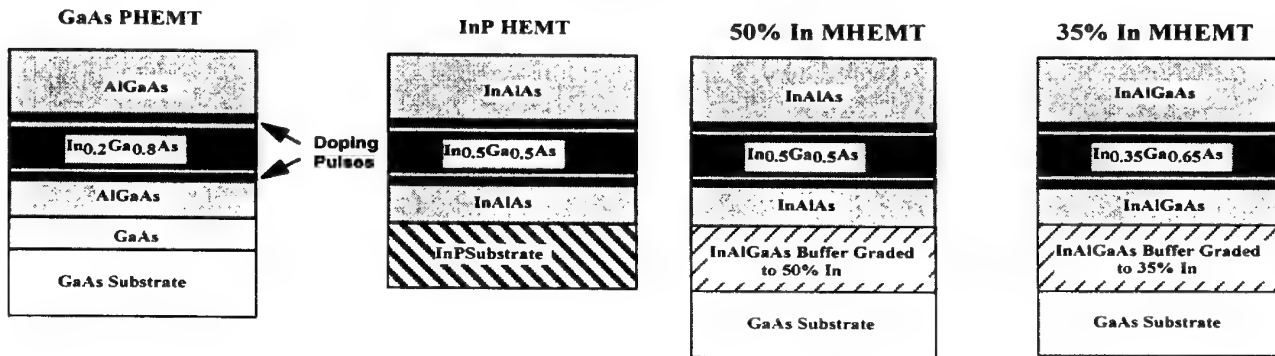


Figure 2: Schematic cross section GaAs pHEMT, InP HEMT and GaAs MHEMT layer structures.

Figure 3 illustrates the superior noise performance of the GaAs MHEMT when compared to the production GaAs pHEMT. As anticipated the noise performance improves with increasing In content. The noise performance advantage of the MHEMT increases with frequency due to the higher  $f_t$  of the MHEMT devices. The noise performance of the MHEMT with 60% In channel is comparable to the best InP HEMT noise performance. In addition, the low noise figure of the MHEMT is achieved over a wide range of drain bias conditions providing for more flexibility in LNA design. The MHEMT also exhibits excellent linearity (high IP3) at low drain current resulting in state-of-the-art values of Linearity Figure Of Merit (LFOM=IP3/Pdc) (see Figure 4). On-state breakdown voltage increases with decreasing channel In content, therefore, by tailoring the channel In content and thickness, the device designer has the freedom to trade off noise performance with operating bias and device robustness.

The low noise, high gain, excellent linearity and low DC power consumption of the MHEMT coupled with the manufacturability of GaAs made the MHEMT an excellent candidate for cost sensitive, high performance applications. Currently at Raytheon, MHEMT LNAs are being designed and fabricated for a wide variety of applications. An example is shown in Figure 5. This 3 stage LNA exhibits <1.7 dB noise figure and  $26 \pm 2$  dB associated gain over a 26 - 32 GHz band while consuming only 31 mW of DC power - a significant improvement in performance over the LNA presented in Figure 1. Unlike the pHEMT LNA, the MHEMT LNA meets and exceeds the requirements of next generation communication systems.

| Structure/<br>Substrate | Channel<br>In(%) / Å | 300K Sheet<br>( $10^{12} \text{ cm}^{-2}$ ) | 300K Mob.<br>( $\text{cm}^2/\text{Vs}$ ) | 77K Sheet<br>( $10^{12} \text{ cm}^{-2}$ ) | 77K Mob.<br>( $\text{cm}^2/\text{Vs}$ ) |
|-------------------------|----------------------|---|--|--|---|
| DPD PHEMT/GaAs          | 20/110               | 3.2   | 6600                                     | 3.2  | 16,000                                  |
| DPD MHEMT/GaAs          | 32/150               | 3.4   | 7500                                     | 3.4  | 23,000                                  |
| DPD MHEMT/GaAs          | 43/150               | 3.4   | 8600                                     | 3.4  | 26,000                                  |
| SPD MHEMT/GaAs          | 60/200               | 3.3   | 10,460                                   | 3.2  | 34,100                                  |
| SPD InP HEMT/InP        | 60/200               | 3.3   | 10,440                                   | 3.2  | 33,900                                  |

**Table 1 Comparison of transport properties of GaAs pHEMT, InP HEMT and GaAs MHEMT with different channel In content**

#### Conclusion

The GaAs MHEMT provides a low cost, high performance alternative to InP HEMT and GaAs pHEMT technology and is the next step in the evolution of GaAs low noise FET technology. As presented above, the GaAs MHEMT offers arbitrary channel In content and therefore provides an additional degree of freedom in device and circuit performance optimization. The GaAs MHEMT is an excellent candidate for meeting the performance requirements for next generation LNAs.

#### Acknowledgements

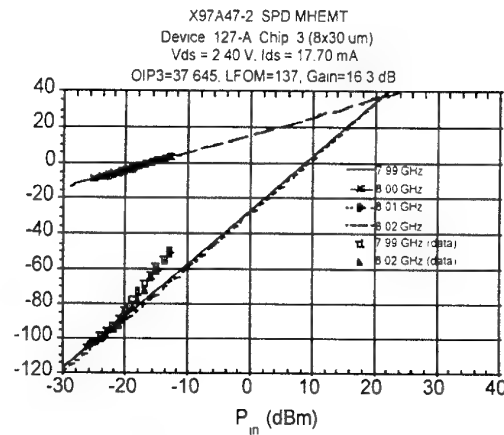
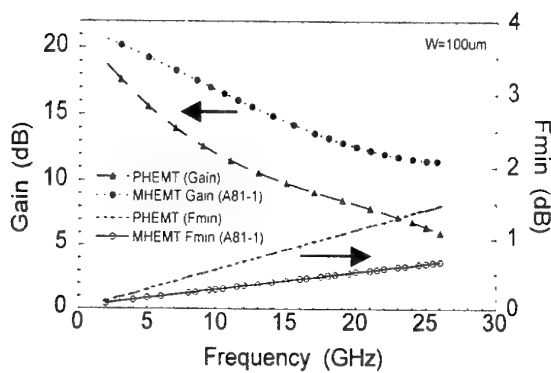
The author would like to acknowledge the contributions of the MHEMT development team at Raytheon - Bill Hoke, Peter Lemonias and Peter Lyman for MHEMT material growth and development; Phil Marsh and Colin Whelan for MHEMT device development; Steve Lardizabal, Rob Leoni and Anette Bowlby for MHEMT noise and linearity characterization and modeling; and Sukchan Kang for MHEMT circuit design.

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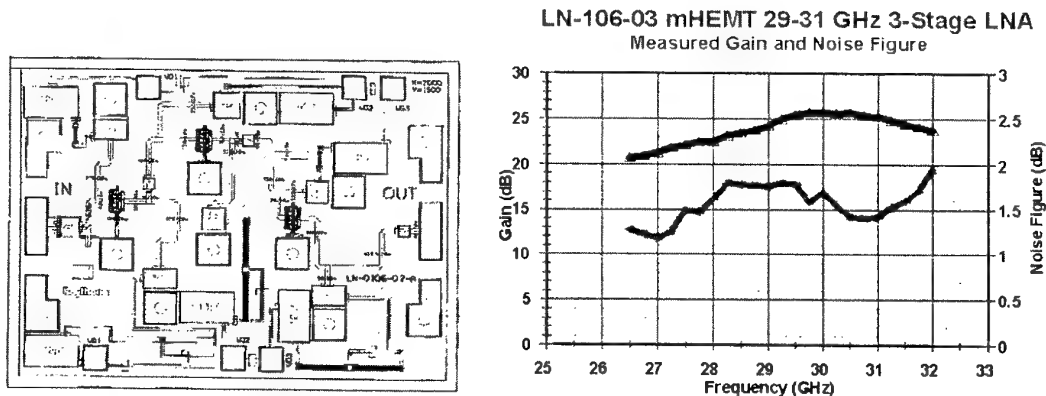
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**Figure 3 (left): Plot of  $F_{min}$  and Associated gain versus frequency GaAs pHEMT and GaAs MHEMT. GaAs MHEMT noise performance is superior to GaAs pHEMT and comparable to InP HEMT.**

**Figure 4 (right): Plot of  $P_{out}$  versus  $P_{in}$  for fundamental signal and third order products. 37dBm IP3 and a Linearity Figure Of Merit ( $LFOM = IP3/Pdc$ ) of 137 was achieved.**



**Figure 5: Plot (right) of  $F_{min}$  and Associated Gain versus frequency for a state-of-the-art 3 stage GaAs MHEMT millimeter wave LNA (left).**

## A 94-GHz CPW Low Noise Amplifier on InP

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### ABSTRACT :

*We present a high performance 2-stage 0.1  $\mu\text{m}$  gate-length InGaAs/InAlAs/InP LM-HEMT MMIC low noise amplifier in coplanar technology. The T-gate profile is realized using silicon nitride  $\text{Si}_3\text{N}_4$  technology leading to naturally passivated devices. We obtain a maximum intrinsic transconductance  $G_m$  of 1600 mS/mm and an intrinsic current gain cutoff frequency  $F_c = 220$  GHz for a drain-to-source current  $I_{ds} = 350$  mA/mm. The extrinsic current gain cut-off frequency  $F_t$  is 175 GHz. At 94GHz, the LNA demonstrates a minimum noise figure of 3.3dB with an associated gain of 12dB.*

### INTRODUCTION:

Low noise amplifiers are essential elements for applications such as LMDS, LANs, satellite constellations as well as passive imaging systems. In the millimeter wave range GaInAs/AlInAs/InP material based transistors are being used increasingly as alternative to PM-HEMT on GaAs. The high cutoff frequency and low noise figure makes InP-based HEMT's very suitable for applications in W-band. In this paper, we report the fabrication and the performance of W-band monolithic 2-stage low noise amplifier based on lattice-matched HEMT devices. The gate process is especially developed for millimeter wave integrated circuits in W-band using coplanar waveguide technology.

### DEVICE PROCESSING

The MMIC amplifier was fabricated on lattice-matched InAlAs/InGaAs HEMT active layer grown by molecular beam epitaxy in our laboratory using a solid source MBE 2300 Riber system. This structure consists of an InAlAs buffer layer, an undoped InGaAs channel, an InAlAs spacer, a single Si planar doping layer, an InAlAs schottky layer and finally a heavily doped InGaAs cap layer. At room temperature, the square resistance is 190  $\Omega/\square$ , the sheet carrier density is  $3.5 \cdot 10^{12} \text{cm}^{-2}$  and the electron mobility is  $9600 \text{cm}^2/\text{V}\cdot\text{s}$ . At 77K, the square resistance is 60  $\Omega/\square$ , the sheet carrier density is  $3.45 \cdot 10^{12} \text{cm}^{-2}$  and the electron mobility is  $32000 \text{cm}^2/\text{V}\cdot\text{s}$ .

The processing steps were optimized to provide high performance and high yield. The devices are isolated using mesa etching with a  $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  solution. To prevent gate-leakage current problems we selectively etch the InGaAs channel at mesa sidewalls with SA (succinic acid): $\text{H}_2\text{O}_2$  solution. Ohmic contacts are realized by evaporating Ni/Ge/Au/Ni/Au metal followed by a  $310^\circ\text{C}$ , 60s, rapid thermal annealing under  $\text{N}_2/\text{H}_2$  atmosphere. The device is then covered up with 800Å silicon nitride film deposited by PECVD. This dielectric layer protects the active zone and supports the top of the T-shaped gate and is also used as the dielectric of MIM capacitors. The 0.1 $\mu\text{m}$  gate length footprint is defined by electron-beam lithography using PMMA and  $\text{Si}_3\text{N}_4$  etching using a highly non-isotropic  $\text{CF}_4/\text{CHF}_3$  RIE process. The top of the gate (0.3 $\mu\text{m}$ ) is then defined using a (PMMA-P(MMA-MAA)) bilayer resist. Gate recess is performed in a SA: $\text{H}_2\text{O}_2$  wet etching solution followed by Ti/Pt/Au metal evaporation [1]. A SEM cross section is shown in Fig.1. To avoid backside processing, coplanar waveguide technology is chosen for the passive circuitry. Metallic resistors consist of a 700Å Ti leading to a sheet resistance of 16 $\Omega/\square$ . To define the CPW ground to ground spacing ( $d=70 \mu\text{m}$ ), a trade-off between losses and low dispersion up to the W-band was considered. The line attenuation is about 0.4dB/mm at 94GHz for a 50 $\Omega$  transmission line. Electro plated air bridges were added at each discontinuity to suppress the undesired slot-line mode. The air-bridges were designed to introduce low parasitic effects over the whole W-band. For the amplifier design, an R-L-C-G distributed model was established for each element [2, 3].

### RESULTS

Fig. 2 shows a photo of the complete realized W-band two stage CPW amplifier. The chip size is 1.7mm x 1.5mm. S-parameters noise figure and associated gain of amplifiers were characterized on wafer. The noise figure and associated gain performance measured at 94 GHz are shown in Fig.3 for different amplifiers and biasing conditions. At 94GHz, the best LNA demonstrates a minimum noise figure of 3.3dB with an associated gain of 12dB which is a very good result for a low noise amplifier using coplanar wave guide technology in W band.

### ACKNOWLEDGMENTS

The author would like to thank the French MOD for its financial support under contract 95162-95536.

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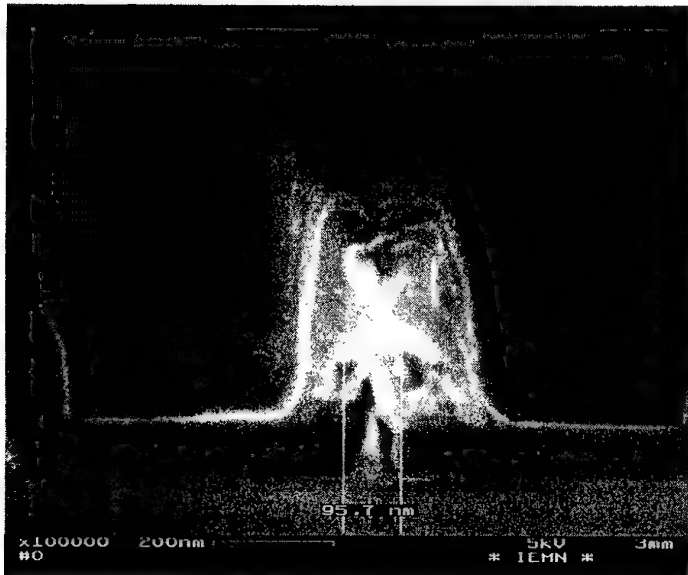


Fig.1. SEM picture of a 0.1  $\mu\text{m}$  gate deposited on the silicon nitride layer.

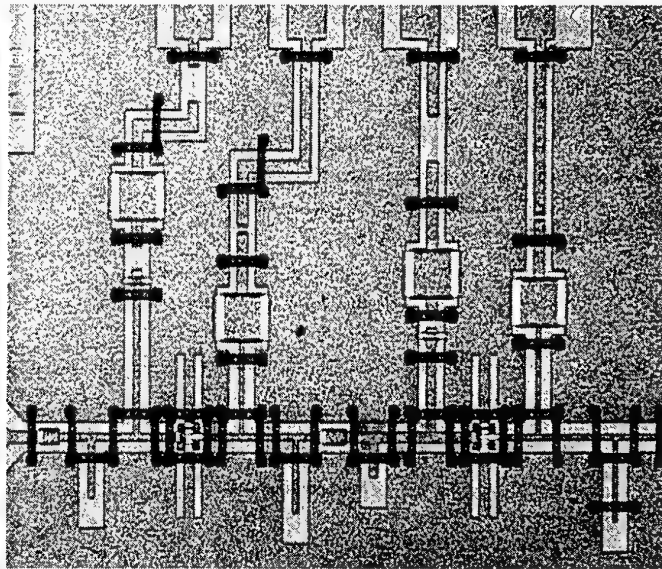


Fig.2. photo of the realized two stage CPW amplifier

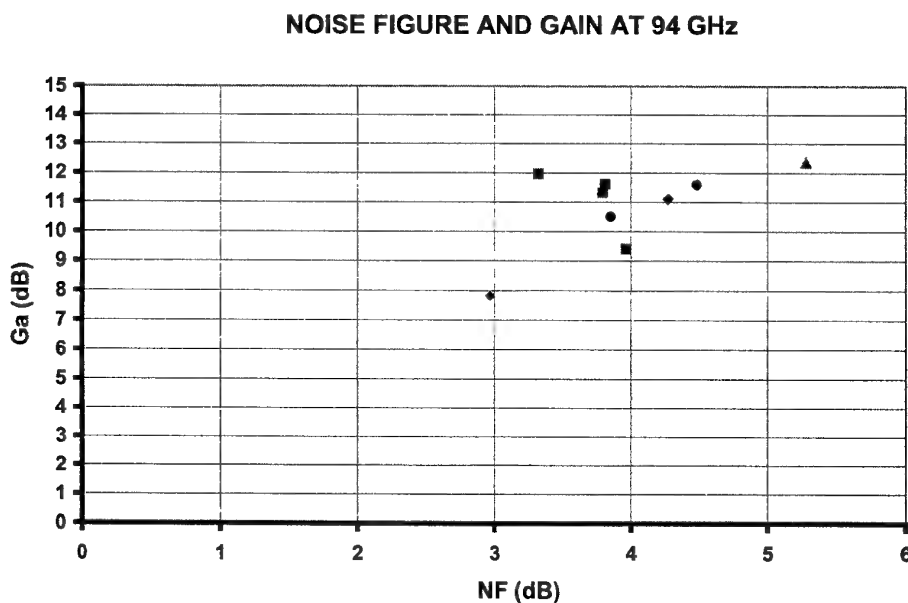


Fig.3. Noise figure and gain measured at 94 GHz for the two-stage CPW amplifier. Uncertainty is about 0.2 dB for both noise figure and gain

## High - Efficiency MMIC Power Amplifiers Using AlGaAs p-HEMT Technology

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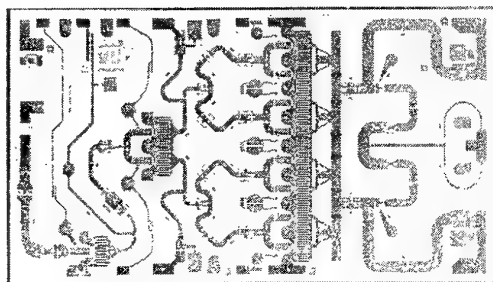
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Power p-HEMT technology has today raised sufficient maturity to be widely used in space borne equipment. Recent developments in the field of MMIC power amplifiers for Ku band applications have been conducted in Alcatel Space Industries using 0.25  $\mu\text{m}$  AlGaAs p-HEMT power technology from TriQuint Semiconductor Texas (TQT). Two Ku-band amplifiers delivering more than 2 and 4 W output power respectively for active antenna applications have been designed with high level performances in terms of efficiency and linearity. A space qualification program including RF step stress and DC life test to demonstrate the ability of this technology to operate during a 15 years flight duration is in progress.

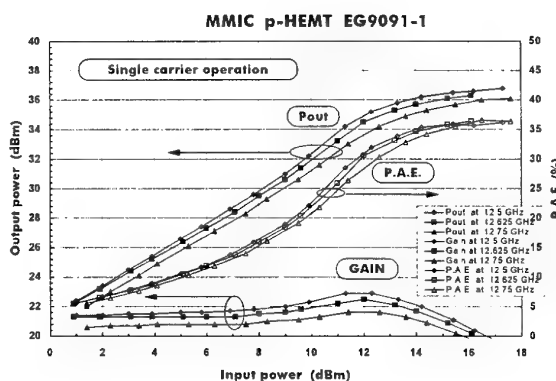
### • Ku-band 4W Amplifier

This 4W output power amplifier (TQT design on Alcatel's specifications) has been developed in the frame of STENTOR program dedicated to the qualification of advanced technologies and concepts (satellite founded by French government). One of the challenges of this technological satellite was to develop a Ku-band transmit active antenna including 48 SSPA able to deliver substantial output power with limited on board power resources.

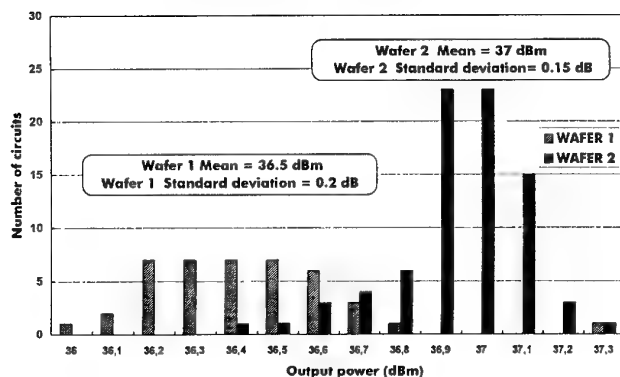
To overcome this challenge and to achieve the best trade-off between antagonist parameters as high output power, low DC consumption and high linearity, the p-HEMT technology appears to be presently the best candidate. The 0.25  $\mu\text{m}$  p-HEMT technology from TQT has been selected to develop the output stages of the SSPA's. A three-stage MMIC power amplifier (EG9091-1) has been designed to operate between 12.5 and 12.75 GHz and to deliver typically more than 36 dBm with 36% P.A.E. in single carrier mode. In multicarrier mode, this chip delivers 33.6 dBm with 30% P.A.E. and 15 dB NPR. The gate peripheries of the 3 stages are 1.25 mm, 3 mm and 12 mm respectively. On-wafer power measurements show low performance dispersion (gain, output power and P.A.E.) on more than 120 chips from 2 wafers.



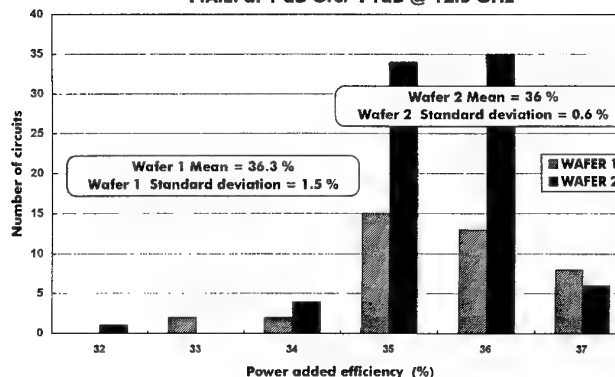
Photograph of 4W Ku-band amplifier (EG9091-1)



PERFORMANCE DISPERSION OF EG9091-1  
OUTPUT POWER at 1 dB G.C. @ 12.75 GHz



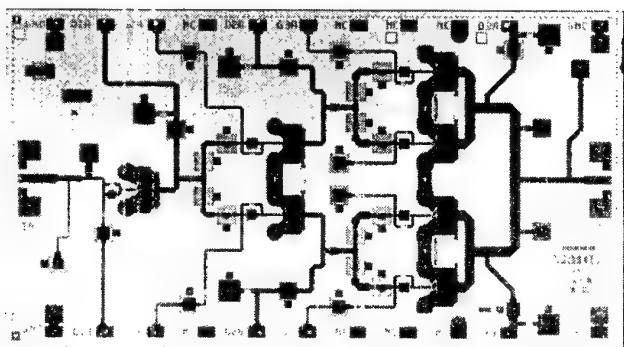
PERFORMANCE DISPERSION OF EG9091-1  
P.A.E. at 1 dB G.C. P1dB @ 12.5 GHz



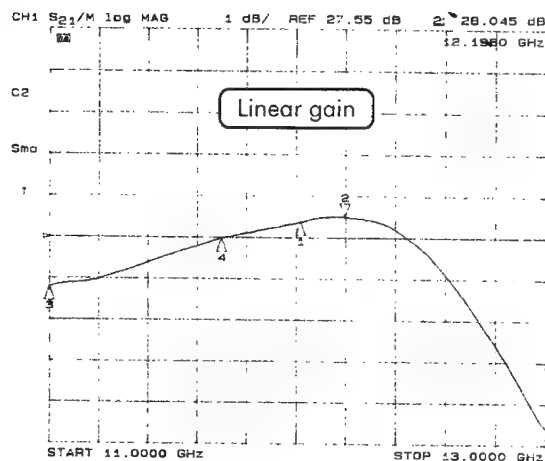
### • Ku-band 2W Amplifier

A 3-stage amplifier (HPATI10A) dedicated to transmit active antenna applications has been designed by Alcatel and manufactured by TQT foundry with 0.25  $\mu\text{m}$  p-HEMT process. The gate peripheries of the 3 stages are 0.6 mm, 2.5 mm and 6 mm respectively. Chip size is 3 mm X 5.5 mm. This circuit operates in 11.7-12.2 GHz bandwidth, presents 27 dB linear gain and delivers more than 33.5 dBm with up to 36% P.A.E. in CW mode at about 1 dB gain compression (measurements performed in test fixture with about 0.4 dB output RF losses not deembedded). An ambitious goal in terms of efficiency and linearity in multicarrier operation has been assigned to this circuit in order to satisfy the mission requirements: P.A.E. must be kept better than 22% along with an NPR higher than 15 dB over a 10 dB output power range. This specification along with a double frequency bandwidth represent additional constraints with regard to those of the 4W amplifier. A variable power supply able to deliver a controlled output voltage between 3 and 8 V is coupled to the amplifier in order to be able to decrease the drain voltage versus the input power back-off with the objective to keep the P.A.E. over 22%.

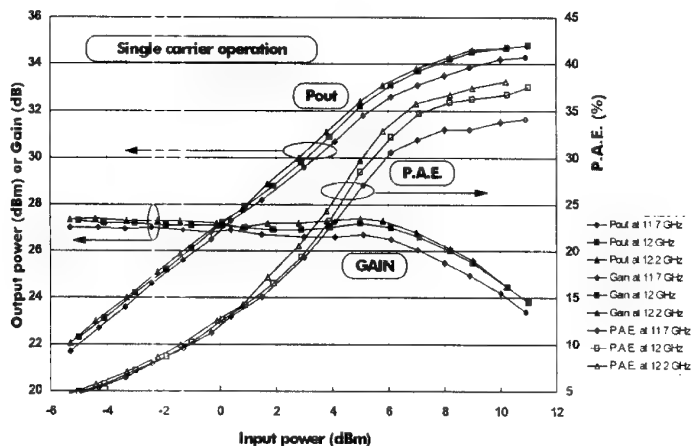
This goal at maximum output power (30 dBm in multicarrier operation) has been achieved over the operating frequency bandwidth. Measurements with variable drain voltage are in progress to determine the behaviour of the circuit over the 10 dB output power range.



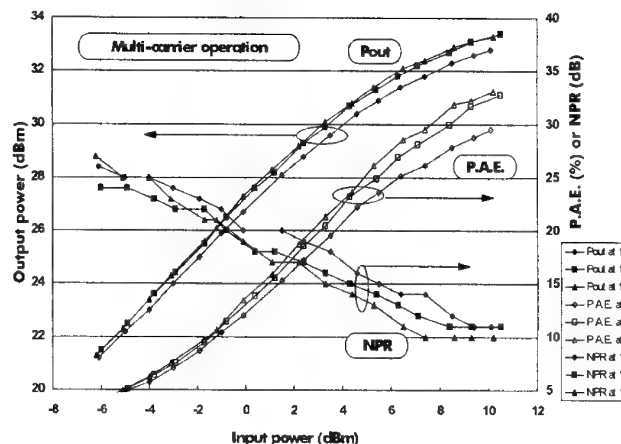
Photograph of 2W Ku-band amplifier (HPATI10A)



MMIC p-HEMT HPATI10A



MMIC p-HEMT HPATI10A



**Acknowledgment:** the development of the Ku-band 4W amplifier has been supported by CNES and France Telecom in the frame of STENTOR program.

## GaAs PHEMT Spice Model for Very High Bit Rate Digital Circuits

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**Introduction** - As the bit rate of digital functions increases up to 40 and 60 Gb/s, enhancement/depletion high  $f_T$  PHEMT technology appears as an attractive solution. Digital functions up to 40 Gb/s have already been demonstrated with a Normally-ON/Normally-OFF GaAs PHEMT process, with  $0.2\mu\text{m}$  gate length and 65 GHz Transition Frequency [1]. The extension of this technology, by further reducing the gate length from 0.2 to  $0.15\mu\text{m}$ , is under developpement, with the expectation of a 75 GHz transition frequency. However, accurate modelling and simulation of high bit rate digital functions has to face specific problems. This paper presents a specific Spice model for the simulation of digital functions for operating frequencies from DC up to 65 GHz.

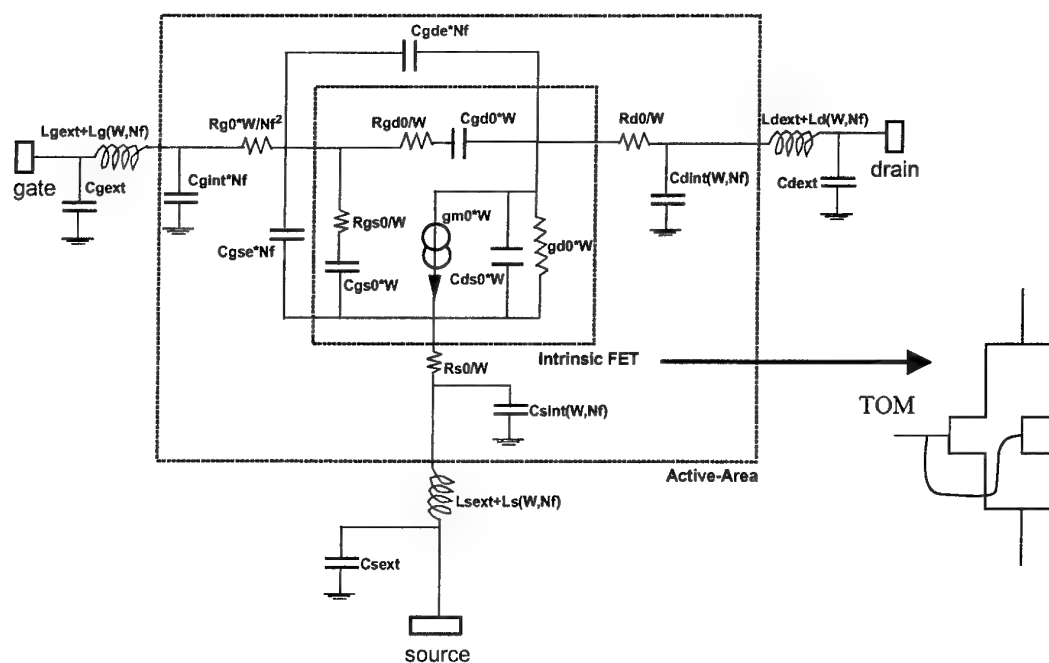
**Parasitics extraction and scaling** - For very high frequency applications, access parasitics and capacitances to ground are critical simulation elements. Accurate extraction and scaling of parasitics has to be considered the preliminary and necessary condition for large-bandwidth modelling. The complete measured FET equivalent circuit we propose is given in **figure 1**. All parasitics elements are directly derived from measurements performed at  $V_{ds}=0$  (cold FET) [2].  $L_{gext}$ ,  $C_{gext}$ ,  $L_{dext}$ ,  $C_{dext}$ ,  $L_{sxt}$ ,  $C_{sxt}$  are the parasitic elements of the coplanar test pads. As far as they do not depend on FET dimensions, these elements can be defined as the constant parts of the extracted inductances or capacitances.  $L_g$ ,  $L_s$  and  $L_d$  are the access inductances of the FET, leading to the Active-Area-FET. The Active-Area-FET can be defined as the transistor without parasitic access elements. In digital circuits, layout tends to be as compact as possible, so the Active-Area-FET is most of the time the transistor cell to be considered for simulation.  $C_{gse}$  and  $C_{gde}$  are the interelectrode capacitances,  $C_{gint}$ ,  $C_{dint}$  and  $C_{sint}$  capacitances to ground of the active-area (calculated using the perimeter and area of the gate, source and drain contacts).

**PSpice model** - As far as Spice simulator is specifically devoted to simulations of digital circuits, the development of a PHEMT large-bandwidth Spice model can be considered an important tool. However, the specific PHEMT  $g_m(V_{gs})$  characteristic cannot be simulated by the MESFET classical models given by Spice. This problem can be solved by the association of two TOM (PSpice GaAsFET LEVEL 5) cells in parallel (see **figure 1**). The global drain-source current is the sum of the drain-source current of the two TOM cells. Assuming that the drain current of the second TOM cell is negative and that threshold voltages of the two cells verify  $V_{T02} > V_{T01}$ , this association allows the  $g_m(v_{gs})$  to exhibit a maximum value. This model is in good agreement with the  $g_m$  and  $I_{ds}$  data (**figure 2**), all over the practical  $V_{ds}$  range (ohmic or saturated zones).

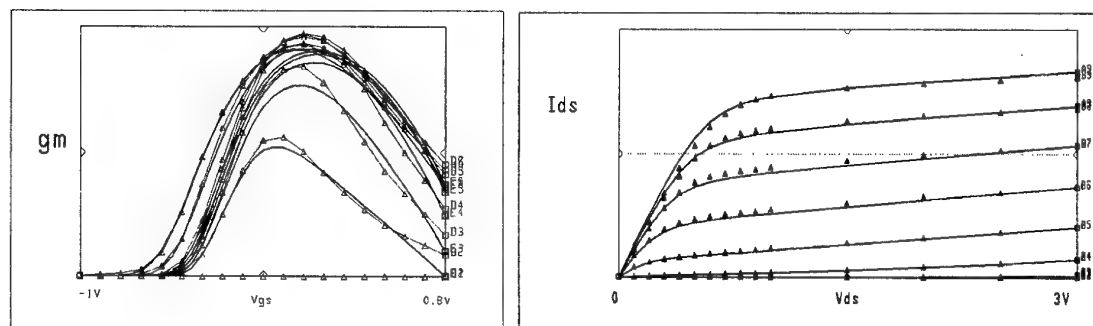
**Results** - There is a good agreement between measured and simulated S-parameters (**figure 3**) up to 65 GHz. However, some limitations have been identified :  $r_{gs}$  and  $r_{gd}$  elements do not appear in the TOM model, thus causing a difference on  $S_{11}$  phase at high frequencies, and variation of  $C_{gs}$  with  $V_{ds}$  given by the TOM model is not always satisfactory.

[1] 40 Gb/s ICs using a production PHEMT technology, J. Hourany and al., GaAs'98, Amsterdam, pp500-503

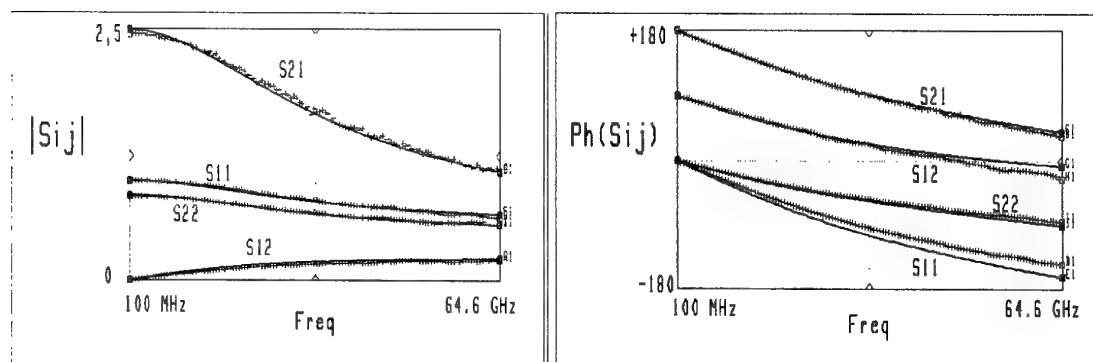
[2] A new method for determining the FET Small-Signal Equivalent Circuit, G. Dambrine and al., IEEE Transactions On Microwave Theory and Techniques, Vol.36 n°7, July 1988



**Figure 1 :** PHEMT complete equivalent circuit with scaling rules (W : total width, Nf : number of fingers)



**Figure 2 :** gm(Vgs) and Ids(Vds) characteristics — Spice model  $\triangle$  measured or extracted data



**Figure 3:** Comparison between measured and simulated S parameters (magnitude and phase) for a 4x15 $\mu\text{m}$  transistor biased at  $V_{ds}=3\text{V}$ ,  $V_{gs}=0$ .

           simulation      + measurement

# Composite channel InP HEMT for high cut-off frequency $\times$ breakdown voltage performance

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## Introduction

The high frequency and breakdown voltage performances of composite channel InP HEMT have already been demonstrated [1] and make them very attractive for the monolithic optoelectronic integration. If the breakdown voltage and the cut-off frequency of these devices are high enough, they can be used for optical fiber transmitter applications, for example as driver for an electro-absorption modulator. An important figure of merit is then the cut-off frequency  $\times$  off-state breakdown voltage.

## Device fabrication

The composite channel HEMT structures (A and B) are grown by MOVPE (Fig. 1). The buffer is composed of a thin InAlAs layer grown at 540 °C, which is therefore semi-insulating, while the top is grown at 650 °C [2]. The channels are composed of 100 Å InP (sub-channel) and 100 Å InGaAs layers. For both structures, the InAlAs spacer layer is 40 Å thick with a Si  $\delta$ -doped plane on the top. The AlInAs barrier thickness are 150 Å and 200 Å for structures A and B respectively. The 100 Å InGaAs cap layers are undoped. A standard process has been applied to both structures : GeAuNiAu alloyed ohmic contacts, e-beam lithography of the T-shape gates, wet selective gate recess and TiPdAu metal deposition, mesa chemical etching and interconnection. For structures A and B, Hall measurements give respectively  $n_s = 2.18 \times 10^{12} \text{ cm}^{-2}$  and  $\mu = 9780 \text{ cm}^2/\text{V.s}$ , and  $n_s = 2.24 \times 10^{12} \text{ cm}^{-2}$  and  $\mu = 10200 \text{ cm}^2/\text{V.s}$  at room temperature. Source and drain contact resistances are about 0.44  $\Omega \cdot \text{mm}$  for structure A and 0.18  $\Omega \cdot \text{mm}$  for structure B.

## Results and discussion

Both structures are characterized by static and dynamic measurements. The devices have gate lengths varying from 0.1 to 0.7  $\mu\text{m}$ , and gate-drain distances  $L_{\text{GD}}$  varying from 0.9 to 1.9  $\mu\text{m}$  (Table I). The saturation drain current  $I_{\text{dss}}$ , the extrinsic and intrinsic transconductances  $g_m$  and  $g_{m0}$  for different gate lengths of structure A are shown on Fig. 2. At 0.1  $\mu\text{m}$  gate length, bidimensional effects could explain the decrease of the transconductances.

The evolution of the cut-off frequencies  $f_t$  and  $f_{\text{max}}$  for both structures is shown on Fig. 3. Because of a better gate length to barrier thickness aspect ratio (at  $L_G = 0.1 \mu\text{m}$ ), the frequency performances of structure A are improved with respect to structure B. In spite of a larger source resistance, the thinner barrier permits to reach 165 GHz for  $f_t$  and 285 GHz for  $f_{\text{max}}$ ; this represents an increase of 15 GHz (+10 %) for  $f_t$  and 45 GHz (+18 %) for  $f_{\text{max}}$ .

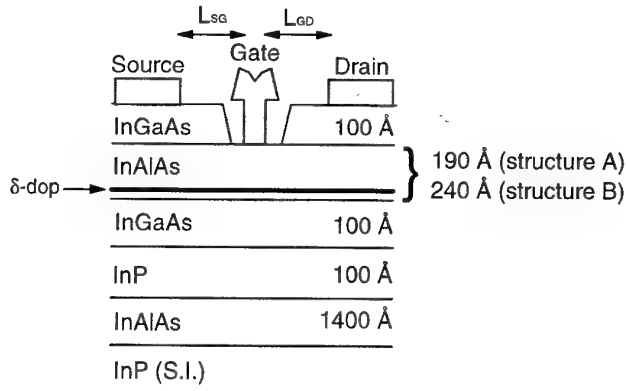
The on-state ( $V_{\text{gs}} = 0 \text{ V}$ ) and off-state ( $V_{\text{gs}} = V_p$ ) breakdown voltages  $V_{\text{BR-on}}$  and  $V_{\text{BR-off}}$  are measured for 0.1  $\mu\text{m}$  gate length transistors with different gate-drain spacings (Fig. 4). The on-state breakdown voltage is quite independent of the gate-to-drain spacing  $L_{\text{GD}}$ . However it is influenced by the AlInAs barrier thickness which tends to increase  $V_{\text{BR-on}}$  when it is higher because of the reduced tunnel electron current [3][4]. But the off-state breakdown voltage is very dependent on  $L_{\text{GD}}$ . This confirms that the phenomenon appears at the drain edge of the gate where the electric field is the highest [5]. This effect is more sensitive for  $L_{\text{GD}}$  above 1.2  $\mu\text{m}$ . For a  $L_{\text{GD}}$  of 1.9  $\mu\text{m}$ ,  $V_{\text{BR-off}}$  increases from 7 to 14 V when the barrier is 50 Å thicker. The microwave frequency performances are shown on figure 5, where  $f_t$  and  $f_{\text{max}}$  are represented versus  $L_{\text{GD}}$ . Because of a higher access resistance ( $L_{\text{SG}} \approx L_{\text{GD}}$ ),  $f_t$  is 9 GHz lower (-6 %) for  $L_{\text{GD}} = 1.9 \mu\text{m}$ , and because of a considerable decrease of the output conductance  $g_d$  from 100 to 55 mS/mm, the improvement of  $f_{\text{max}}$  is about 55 GHz (+25 %).

## Conclusion

In order to optimize the composite channel HEMT structure, the barrier thickness and the gate-drain spacing have been varied. Depending on the application, there is a compromise between cut-off frequency and breakdown voltage. A thinner AlInAs barrier permits to improve the cut-off frequency with a degradation of the off-state breakdown voltage. Conversely, breakdown voltage can be improved with a larger gate-to-drain spacing with only a slight loss in dynamic performances.

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 [3] S.R. Bahl *et al.*, Proc. of the 6<sup>th</sup> IPRM, 1994, 243.  
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 [5] M. Matloubian *et al.*, Proc. of the IEEE IEDM Tech. Digest, 1993, 915.



| $L_{SG}$ ( $\mu\text{m}$ ) | $L_{GD}$ ( $\mu\text{m}$ ) |
|----------------------------|----------------------------|
| 0.9                        | 0.9                        |
| 1.1                        | 1.2                        |
| 1.4                        | 1.4                        |
| 1.4                        | 1.9                        |

Table 1  $L_{SG}$  and  $L_{GD}$  spacing

Figure 1 MOVPE HEMT structures

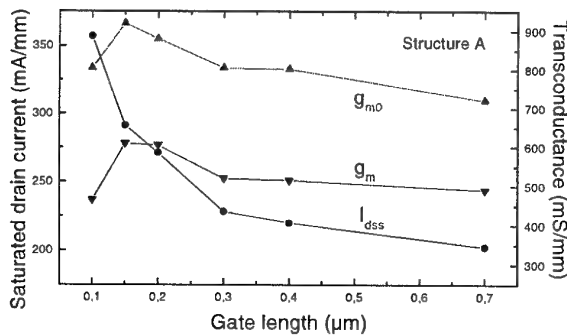


Figure 2 Saturation drain current  $I_{dss}$ , extrinsic and intrinsic transconductances  $g_m$  and  $g_{m0}$  versus gate length for structure A.

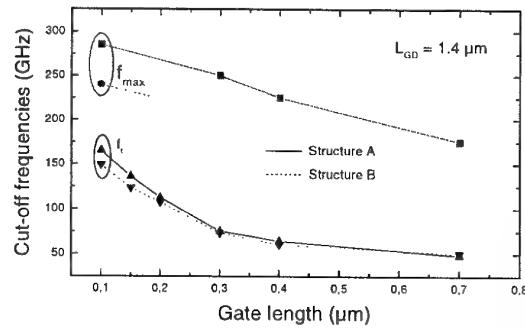


Figure 3 Current gain cut-off frequency  $f_b$  and power gain cut-off frequency  $f_{max}$  versus gate length for structures A and B.

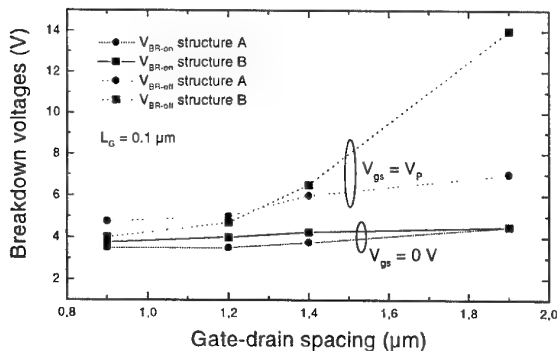


Figure 4 On-state and off-state breakdown voltages  $V_{BR-on}$  and  $V_{BR-off}$  versus gate-drain spacing of 0.1  $\mu\text{m}$  gate length transistors for structures A and B.

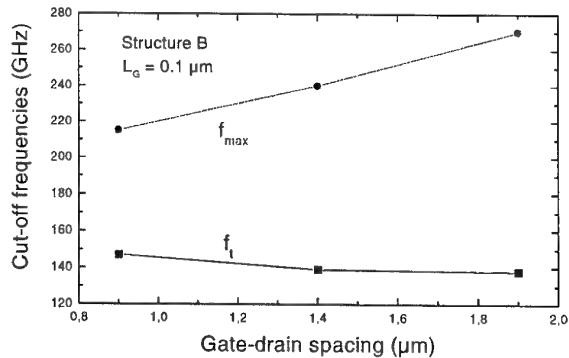


Figure 5 Current gain cut-off frequency  $f_i$  and power gain cut-off frequency  $f_{max}$  versus gate-drain spacing of 0.1  $\mu\text{m}$  gate length transistors for structure B.

## CHARACTERIZATION OF RESIDUAL CARBON IN SEMI-INSULATING GaAs SUBSTRATES FOR INTEGRATED CIRCUITS

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The quality of GaAs based integrated circuits depends strongly on the carbon content as it influences the properties of gallium arsenide substrates. Really, the carbon atoms could change the substrate conductivity and its thermal stability, the EL2 defect compensation, the substrate electrical uniformity and so on. The report is dedicated to a critical analysis of the existing data about the carbon effect on the GaAs electrical properties. Some new ways to characterize the carbon effect on the quality of GaAs based integrated circuits will be proposed.

Thursday, May 27, 1999 09:00 am

## Optoelectronic 2

- *PBG in two-dimensions : from concepts to applications (invited paper)* p. 87  
 Henri Benisty, D. Labilloy, C. Weisbuch, T.F. Krauss<sup>(1)</sup>, C.J.M. Smith<sup>(1)</sup>, R.M. De La Rue<sup>(1)</sup>,  
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 Ecole Polytechnique-LPMC, Palaiseau, France  
<sup>(1)</sup> University of Glasgow, Glasgow, UK  
<sup>(2)</sup> EPFL, Lausanne, Switzerland
- *High Q-factor 2D photonic bandgap microcavities on InP-based suspended membranes* p. 91  
 P. Pottier, C. Seassal, X. Letartre, J.L. Leclercq, P. Viktorovitch, D. Cassagne<sup>(1)</sup>, and C. Jouanin<sup>(1)</sup>  
 Ecole Centrale de Lyon-LEOM, Lyon, France  
<sup>(1)</sup> University of Montpellier-GES, Montpellier, France
- *Responsivity enhancement in GaInAs/InAlAs/InP OPFETs by backgating* p. 93  
 U. Hodel, M. Marso, A. Fox, A. Förster, and P. Kordos  
 Institute of Thin Film and Ion Technology, Jülich, Germany
- *Design and first results on a vertical integrated transistor-laser structure for high-speed low-chirp modulation* p. 95  
 R.C.P. Hoskens, B. Ljevar, G. Archontopoulos, V.I. Tolstikhin, and T.G. van der Roer  
 Technische Universiteit Eindhoven, Eindhoven, Netherlands
- *Investigation of a PIN laser cleaved surface using Kelvin probe force microscopy and 2D physical simulations* p. 97  
 F. Robin, H. Jacobs, O. Homan, A. Stemmer, and W. Bächtold  
 ETH Center, Zurich, Switzerland

# Photonic Band Gap in two-dimensions : from concepts to applications

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**Abstract :** The applicability of the concept of photonic band gap (PBG) materials, also called Photonic Crystals (PC) to optoelectronic devices is discussed in the two-dimensional (2D) case. Combination of conventional waveguiding with 2D-PC for lateral structuration is assessed by means of transmission/reflection/diffraction measurements making use of luminescence of built-in active layers. High-Q confined modes in PC-bounded "in-plane" microcavities are then demonstrated.

**INTRODUCTION :** Photonic crystals (PCs) are structured materials with a strong periodic modulation of the dielectric constant in two or three dimensions. In 2D, they may exhibit a photonic band gap (PBG) in any in-plane direction in a sizable frequency range [1] for peculiar lattices and simple structurations e.g. cylindrical holes on a triangular lattice. This "light insulator" behaviour relies on a stronger mechanism than the usual total-internal reflection (TIR) and makes these PC privileged candidates for novel guide boundaries allowing ultimately sharp bends and also to define in-plane optical cavities [2]: as well as more complex functions [3].

**DESIGN AND TEST OF BASIC PCs :** What is a basic PC for integrated optics purpose ? A triangular array of holes perforating a planar semiconductor waveguide is a preferred realization [4]. Typical lattice spacing are in the 200–400 nm range with diameters of 120–300 nm and depth of  $\sim 1 \mu\text{m}$  in order to overlap the guided mode profile (Fig.1). An important issue is to diminish the hole diameter to minimize scattered light out of the guide [5,6]. As a result, PCs feature an omnidirectional bandgap only for the TE polarization.

The optical properties of PCs were probed in the configuration of Fig.2a, whereby guided photoluminescence of InAs self-organized dots grown inside the guide forms a convenient internal source, light being collected at a cleaved edge [7,8,9]. Transmission oscillations around the band edge of a 15 rows-thick PC, Fig.2b, indicate that waves achieve full round-trips across the crystal with moderate losses, in spite of the numerous holes traversed by the wave.

From this initial success, the use of PCs in lateral guides raises two kinds of issues. The lateral guiding by PCs is a matter of opened debate : is it possible to achieve efficient waveguiding on sizable distances ? No attempt has been made yet to evaluate the answer from the above data, let alone direct measurements. The second issue is related to the introduction of PCs in present integrated-optics devices with conventional guide sections. PC-based components such as prisms or splitters might play a role in this respect [10].

**MICROCAVITIES - Fabry-Pérot Microcavities.** As they rely on multiple reflections, horizontal cavities bounded by PCs are useful test structures for resonant devices. We recently fabricated and tested PC-based Fabry-Pérot cavities, each mirror consisting of 4 rows crystals (inset of Fig.3), with a TE gap around  $1 \mu\text{m}$  [11]. Transmission spectra across such cavities with a

variable submicronic spacer are shown in the graphs of Fig.3. The peak wavelength vs. spacer thickness follows the theoretical prediction of Fig.4 [12]. This suggests that the deterministic placement of a defect mode into a PC is a feasible task. Here, we found Q's in excess of 100 for cavity orders  $m < 3$ , which translate into finesses  $F \approx 30$  and reflectivities  $R \approx 90-95\%$  for each mirror.

- *Micro discs and micro hexagons.* Fully confined "in-plane" micro-cavities raise the issue of the mirror's directionality. Micro-discs with "whispering gallery modes" have pioneered this area. We attempted to take advantage of concentric Bragg grating to confine different microdisc modes of Fig.5a, denoted "quasi-radial modes" (low azimuthal orders). We fabricated discs of about  $3 \mu\text{m}$  inner diameter, with  $600 \text{ nm}$  spaced trenches [13]. A laser is now focused into the cavity and spontaneous emission of photopumped InAs dots is channeled into the horizontal disc modes. We found that light scattered towards air by the concentric trenches contained the modes spectral information, in the form of sharp peaks with Q's up to 1000. Fig.5b shows such a spectrum in which the peaks were unambiguously identified as quasi-radial modes [13].

We now turn to micro-hexagons bounded with a PC crystal of  $a = 0.24 \mu\text{m}$  period and whose side is only a few  $a$ . The hexagon shape is naturally carved into a triangular crystal. Using PC boundaries results in a confinement of all guided radiations [14,15]. Some results for a  $5a$ -side cavity are shown in Fig.6. From top to bottom, we show the light collected on the front surface of the sample for different location of the excitation and the detection. Fig.6a is for both excitation and detection in the same unetched area, which is the usual PL of InAs dots. Fig. 6b is for excitation and detection both inside the hexagonal cavity. PL is attenuated but some sharp peaks emerge above the continuum. Fig.6c shows that only these peaks survive or even grow when detection at the PC boundary is performed. Simulations of this kind of modes will be shown to understand the observed features.

Finally, from the properties of these objects, we can expect two classes of applications : (i) in integrated optics, waveguide and the implementation of functionalities based on resonant structures such as Add-Drop filters could take advantage of the compactness of PC-based approaches. Bounding conventional stripe lasers by PCs of selected reflectivity, etc.. could also provide novel forms of beam control. (ii) For high-efficiency light sources, the fully confined discrete modes with small volume of e.g. our micro-hexagons, may help accelerating spontaneous emission owing to a sufficiently strong "Purcell effect". At a more basic level, to enhance the efficiency of simple quantum well-based LEDs of larger size, recycling of guided modes owing to the reflecting properties of PCs is also actively sought, especially in the frame of the ESPRIT project SMILED, the support of which is gratefully acknowledged here.

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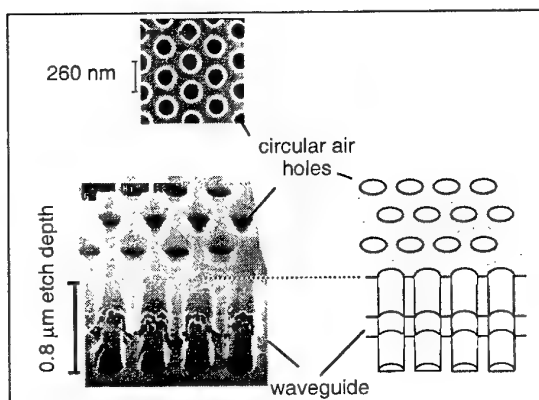


Fig.1 : Top and side view of a photonic crystal of period  $a = 260$  nm consisting of  $160$  nm diameter holes etched through a GaAlAs waveguide with a  $0.8 \mu\text{m}$  etch depth. A photoluminescent layer (e.g. InAs quantum dots) may be included into the waveguide.

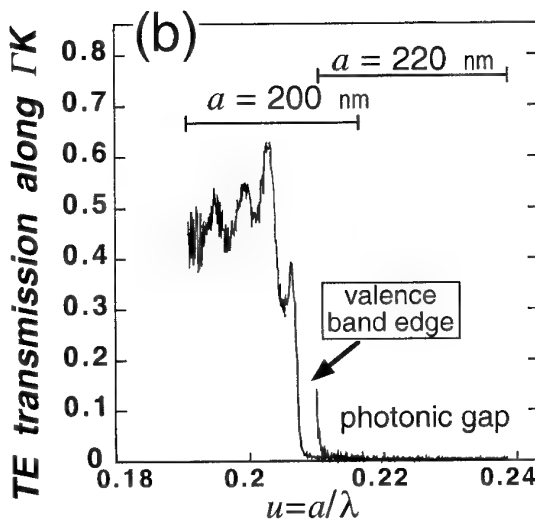
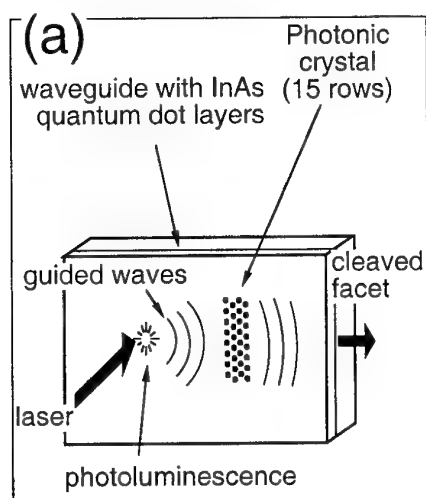


Fig.2 : (a) Experiment principle (b) Stitched normalized transmission along two 15-rows-thick photonic crystals of periods  $a = 200$  nm and  $a = 220$  nm along the  $\Gamma K$  crystal axis. The abscissa is the reduced frequency  $a/\lambda$ .

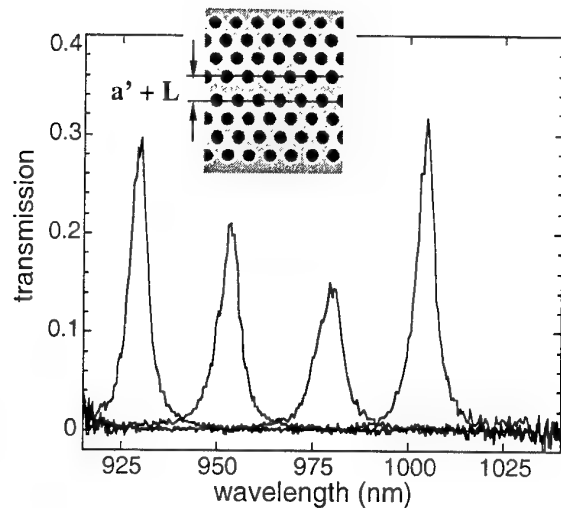


Fig.3: inset : Fabry-Perot cavity consisting of two PC-based mirrors, each 4 rows thick, separated by a spacer of width  $L$  ; graph : Typical set of cavity transmission spectra for cavity spacers  $L=320, 340, 360$  and  $380$  nm

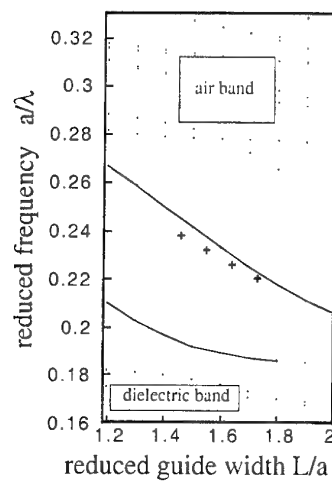


Fig.4 : Comparison of the theoretical prediction of the "defect" mode reduced frequency as a function of spacer width with the measured peak position .

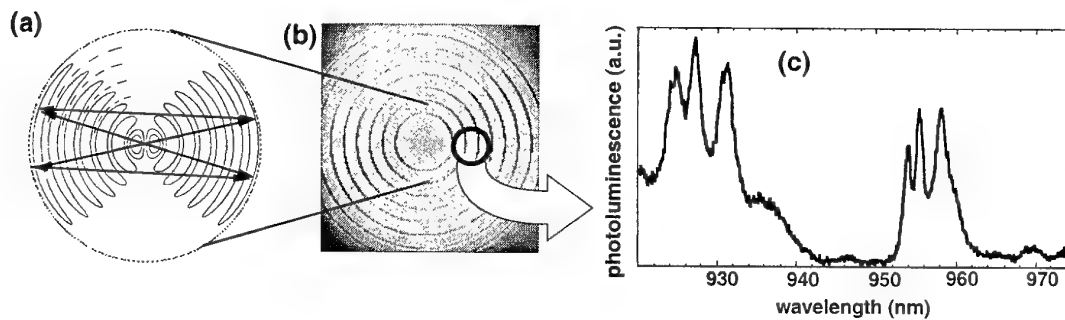


Fig.5 : (a) Sketch of a "quasi-radial modes" in a microdisc (amplitude contours) ; the arrows schematize the equivalent ray trajectory ; (b) micrograph of a microdisc cavity using a concentric grating ; (c) Typical spectrum of the InAs photoluminescence excited in the cavity and scattered by the concentric grating when selectively detecting in the indicated black circle of the micrograph.

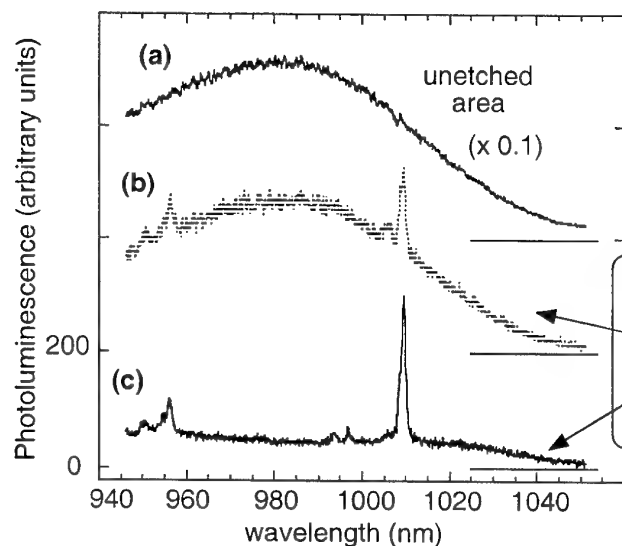


Fig.6 : micro-hexagons : (a) reference PL spectrum of InAs dots for excitation and detection in the same unetched area far from the cavity ; (b) spectrum from an hexagonal cavity of side  $5a$  (inset) for excitation and detection both inside the cavity ; (c) same for excitation inside the cavity and detection just adjacent to the cavity ;

## HIGH Q-FACTOR 2D PHOTONIC BANDGAP MICROCAVITIES ON InP-BASED SUSPENDED MEMBRANES

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For applications in the fields of optical telecommunications and interconnects, and specially for wavelength division multiplexing systems (WDM), basic functions such as filters, modulators, sources and photodetectors are needed. To realize such devices with typical dimensions in the micronic range one of the most promising solutions are to use photonic bandgap (PBG) crystal-based microcavities<sup>1</sup>. To be compatible with planar waveguides, such structures could be advantageously designed in the two dimensions of the semiconductor layers slab. In addition, the need for monolithically integrated optical source, modulator and/or photodetectors can be satisfied by the use of III-V compound semiconductors.

We present the design, realization and PL characterization of PBG crystals where different types of extended cavity-like defects are included (hexagonal and triangular).

The structures are based on InGaAs membranes. They comprise an indium rich quantum well (QW) that emits a TE polarized (E-field lying in the slab) PL signal at 1.9  $\mu\text{m}$ , surrounded by barriers that emit around 1.65  $\mu\text{m}$ . The PBG crystal is a triangular periodic lattice of holes made in the membrane. The hole radius is 200 nm, for a lattice period of 600 nm, leading to a 1.7-2.1  $\mu\text{m}$  forbidden band. Hexagonal and triangular cavities are made inside the crystal by omitting to etch holes in that area (see figure 1). The optical thickness of the layers are chosen in such a way to minimize the coupling between the QW and the vertically radiated modes for the benefit of the in-plane cavity modes. The latter interfere with the PBG mirror and part of the signal is lost in the holes by diffraction. This loss signal is a probe of the behaviour of the cavity.

On figure 2, we compare PL spectra by exciting precisely on a non processed sample, on a suspended membrane, inside the suspended photonic crystal area, and on a suspended PBG cavity.

The unprocessed sample exhibits two spectra that will be considered as references, one for the QW at 1.9  $\mu\text{m}$ , one for the barrier at 1.65  $\mu\text{m}$ . For the membrane, the intensity of the former is lowered while the barrier spectrum is not strongly inhibited. When the laser is focused onto the photonic crystal, the barrier signal is just warped while the QW one is still more inhibited, indicating the existence of a photonic forbidden gap for wavelengths above 1.8  $\mu\text{m}$ . For the PBG cavity on the membrane, in place of the QW spectrum, three peaks, spectrally well resolved, appear with intensities higher than in the reference QW spectrum. We attribute these peaks to the modes of the PBG cavity, as their wavelength are within the photonic bandgap.

Figure 3 shows a high resolution PL measurement on a cavity. A very high density of modes is observed, which is consistent with calculations performed using an order-N plane wave method approach. It can be noted that the Q-factor of the mode at 2041 nm is at least

<sup>1</sup> E. Yablonovitch, Phys. Rev. Lett., **58**, p 2059 (1987)

900. Such a Q value is, to our knowledge, a record for InP-based PBG cavities. It can be correlated with a minimum reflection coefficient of 99% for the PBG mirror. This result demonstrates that, even for 2D PBG structures with subwavelength thickness, high-grade mirrors can be obtained, with little losses in the vertical direction. This opens the way for the exploitation of PBG concept in integrated optics.

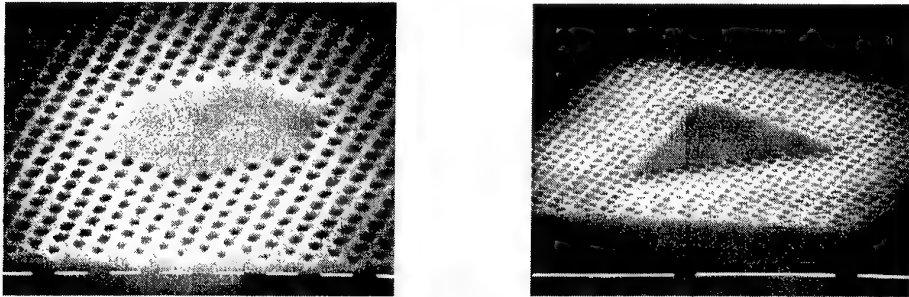


Figure 1 : SEM microographies of the hexagonal and triangular cavities

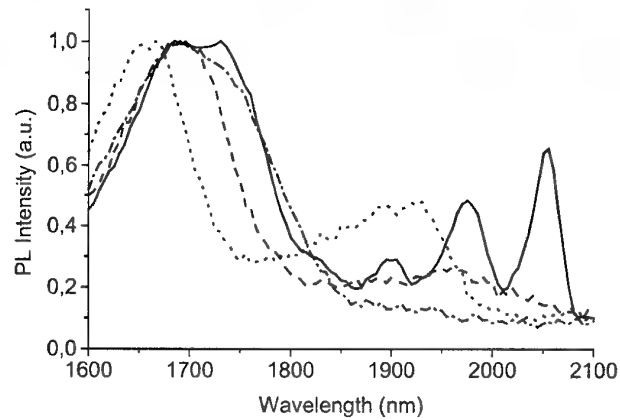


Figure 2 : PL spectra on an unprocessed structure (dotted), on a membrane without PBG (dashed), on the photonic crystal (dotted-dashed) and on a hexagonal PBG cavity (straight)

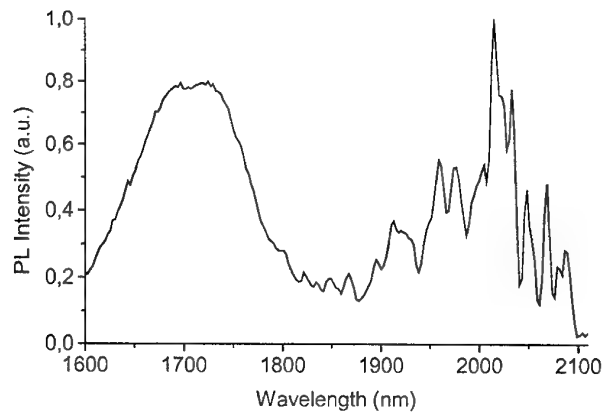


Figure 3 : High resolution PL spectrum on a triangular PBG cavity

## Responsivity enhancement in InGaAs/InAlAs/InP OPFETs by backgating

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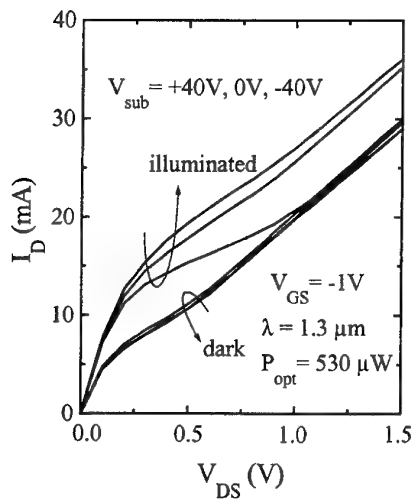
One candidate for a fast optical signal detection for data communication with potential for monolithically integrated circuits is the OPFET [1,2]. We investigated OPFETs, consisting of a pseudomorphic InGaAs/InAlAs system on a semi-insulating double-side polished InP substrate. The typical HEMT structure has an additional 200 nm thick InGaAs absorption layer below the 2DEG for increasing the responsivity of the OPFET. The investigated OPFET has a meander shaped gate and a square layout with an active area of  $50 \times 50 \mu\text{m}^2$ . As previously reported, these OPFETs show a high responsivity of more than 200 A/W [3].

For a better understanding of the physical mechanisms which are responsible for the high DC responsivity, we studied the effect of a voltage, applied to the backside of the substrate. Under optical illumination with a power of 530  $\mu\text{W}$  the DC characteristics show a strong dependence on the polarity and the height of the applied voltage (Fig. 1). A positive voltage of 40 V yields a peak responsivity of 16 A/W (Fig. 2) which is 13 % higher than the responsivity in the zero voltage case. A saturation of the responsivity with increasing substrate voltage can be observed, starting at a voltage of 10 V, so that the responsivity curve in Fig. 2 is within the saturation regime. A negative voltage of -40 V results in a decrease of the peak responsivity of 40 %. We have also observed that at higher drain source voltages, it is possible to suppress the DC photoresponse (Fig. 2). The DC characteristics under dark condition are not significantly influenced by the applied backgating voltage (Fig. 1), which shows that especially optically generated electron hole pairs are responsible for the observed effect.

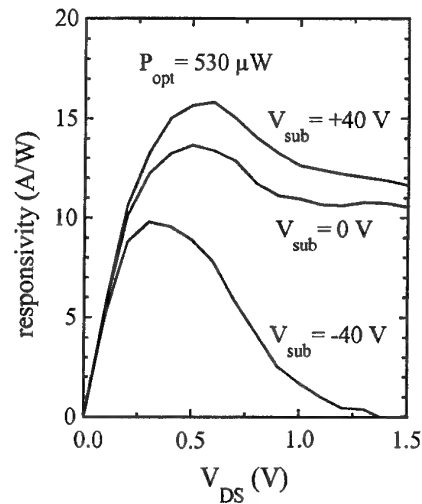
Optoelectronic RF-measurements yield the typical 20 dB/dec slope of the responsivity (Fig. 4), but the backgating voltage changes the responsivity only by approximately 5 % at a frequency of 100 MHz, for both polarities of the voltage, and the effect becomes negligible at higher frequencies. Romero et al. proposed a model for GaAs/AlGaAs OPFETs with two different detection mechanisms. The first component is due to stored holes in the buffer layer that create a so called backgating voltage and is responsible for an extremely high DC responsivity [4]. The second, caused by a direct collection of photogenerated electrons in the 2DEG channel, is responsible for the RF-response.

The first effect also becomes obvious in the dependence of the responsivity from the laser power. Decreasing the laser power leads to a high responsivity of 1000 A/W at a low power of 0.2  $\mu\text{W}$  (Fig. 3). Here the influence of the backgating voltage is obvious, increasing the photoresponse to a value of 1500 A/W by a positive substrate voltage, but decreasing the responsivity more than two orders of magnitude by a negative voltage. Our results, showing a strong effect on the DC responsivity, while the effect on the RF responsivity is negligible are an experimental verification of the two different detection mechanisms. We demonstrate, that also in AlInAs/InGaAs OPFETs a hole storage at the interface of the absorption layer and the buffer layer can be observed.

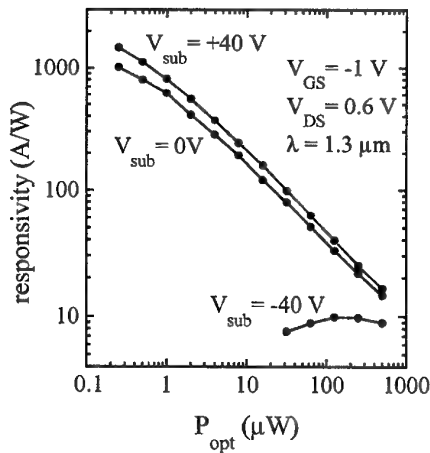
A possible application of this effect might be the tuning of an integrated circuit to reach a higher bandwidth by suppressing the photoresponse at low frequencies or increase the responsivity when a very high photoresponse is needed.



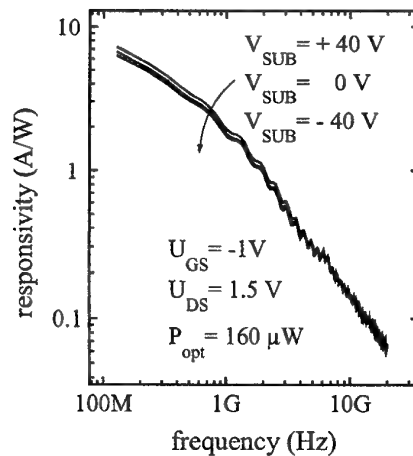
**Fig. 1:** DC-characteristics of an OPFET under optical illumination with varying backside voltage.



**Fig. 2:** DC-responsivity of an OPFET under optical illumination with varying backside voltage.



**Fig. 3:** DC-responsivity as a function of the optical power with varying backgating voltage.



**Fig. 4:** Responsivity as a function of modulation frequency in dependence of different backgating voltages.

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## Design and First Results on a Vertically Integrated Transistor-Laser Structure for High-Speed Low-Chirp Modulation

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### 1. Introduction

The purpose this project is to realise carrier temperature modulation in a laser by means of a novel vertically integrated transistor-laser structure in which the electrons are injected into the active region of the laser via the emitter-base part of a bipolar transistor and heated in a high-field region before entering the active layer.

### 2. Modeling

Since carrier heating effects are critical for this laser the transport problem for electrons travelling over the high electric field region is solved by using the Monte Carlo technique.

In Fig. 1 an example is shown of the results of a Monte Carlo simulation of the part of the device consisting of the GaAs p-doped base, the AlGaAs undoped launcher, the GaAs active region and part of the AlGaAs p-cladding. On the left a so-called scatter plot is shown giving the distribution of carriers in space and energy. Here a two-valley model (Gamma and L valleys) for the conduction band is used. On the right the electron and hole densities are shown. From these results conclusions can be drawn regarding the injection of energy into the AL.

### 3. Device Technology

The structure has been grown by MBE. Processing requires two highly selective wet chemical etching solutions. The [citric acid :  $\text{H}_2\text{O}_2$ ] system shows high GaAs over AlGaAs selectivity. The [ $\text{K}_2\text{Cr}_2\text{O}_7$  :  $\text{H}_2\text{SO}_4$  :  $\text{H}_3\text{PO}_4$  :  $\text{H}_2\text{O}$ ] system on the other hand delivers high AlGaAs over GaAs selectivity. The rest of the processing is conventional.

### 4. Optical measurements

Low-T PL measurements show peaks at 831.1 and 823.6 nm, corresponding to GaAs (active layer), at 803.5 nm, corresponding to AlGaAs with about 3% AlAs mole fraction (base), and at 765.2 nm, corresponding to AlGaAs with 9% AlAs (grading). The launcher (20% AlAs) and p-cladding (20/50 % AlAs) were not seen.

The spontaneous emission of the finished device was smaller than expected and consequently the device showed no laser action. The spectrum at room temperature showed one peak corresponding to an AlAs fraction of 15%, and another peak that varied with bias between 900 and 970 nm. This could come from the base as well as the active layer.

### 5. Electrical measurements

The results of electrical characterisation are shown in Fig. 5. Here bipolar transistor terminology is used, i.e. the p-cladding contact is called "collector. The emitter-base junction operates as expected, however, the "collector" current hardly depends on the emitter but increases linearly with collector-base bias, suggesting that the injected holes do not recombine in the active layer but are injected into the launcher. This would explain the low spontaneous emission from the active layer. The measured characteristics can be very well represented by an adapted HBT model. Together with the spontaneous emission results we conclude that most of the electrons recombine in the base and don't reach the active layer, on the other hand most of the holes overshoot the active layer and end up in the base.

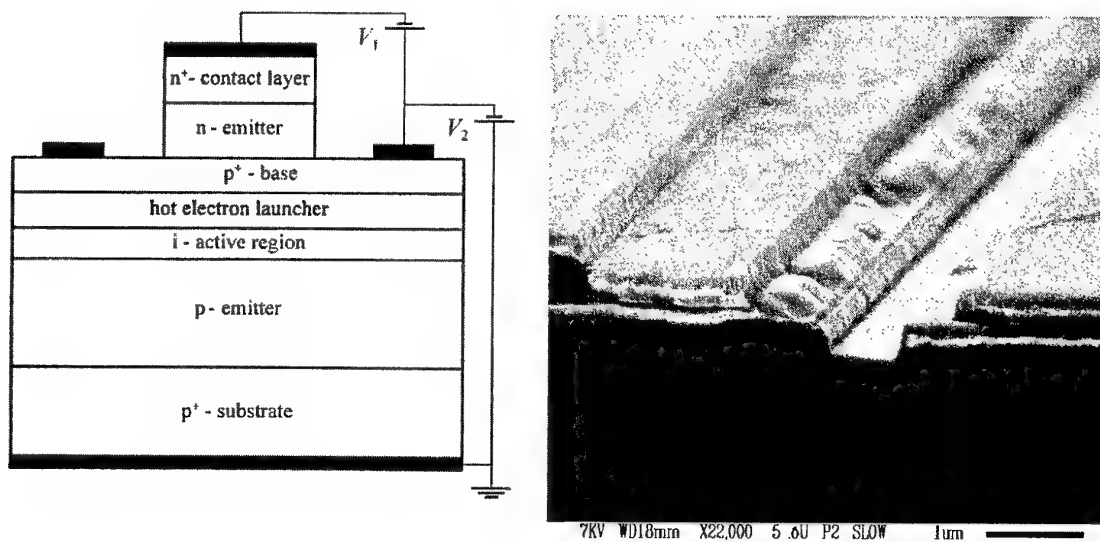


Fig. 1. Cross-section of the hot electron laser and SEM image of the finished structure.

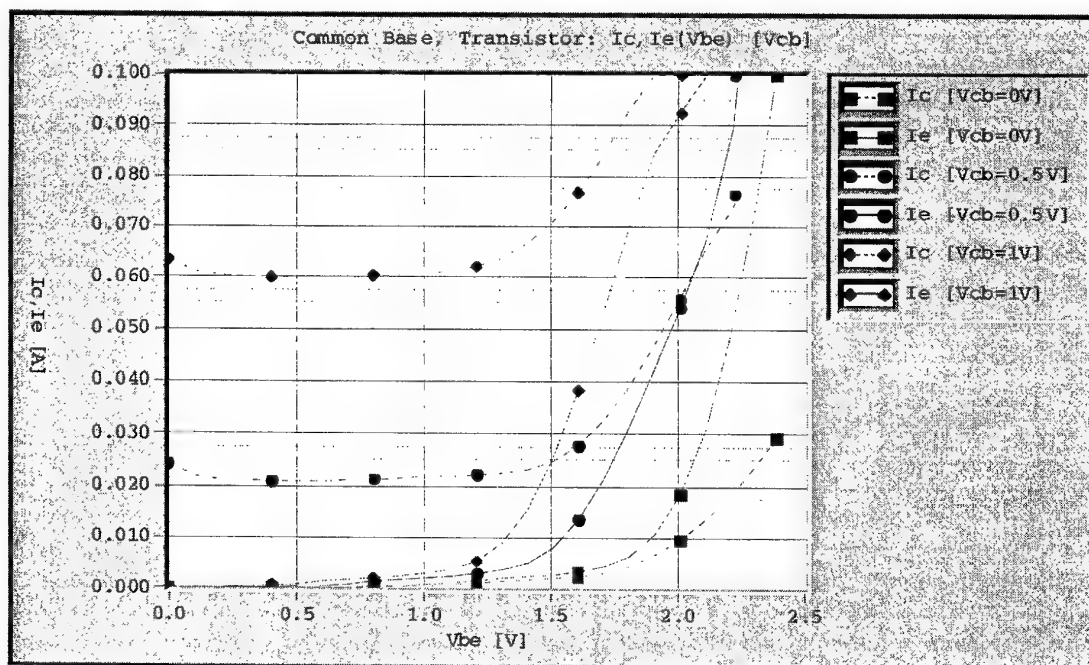


Fig. 2. Current-voltage characteristics at 100 K of the first devices.

# Investigation of a PIN laser cleaved surface using Kelvin probe force microscopy and 2D physical simulations

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## ABSTRACT

We investigated the cross-sectional electric field and potential distribution of a  $n^+$ -InP/InGaAsP/  $p^+$ -InP PIN laser diode using Kelvin probe force microscopy (KFM). KFM results and two-dimensional physics-based simulations were compared and showed excellent agreement. The measured voltage drop between  $n$ - and  $p$ -doped InP regions was 0.4 times smaller than the theoretical value. Our hypothesis that this reduced voltage drop arises from incomplete ionization and surface traps was confirmed by the 2D simulations.

## I. INTRODUCTION

In the past few years, the reduced dimensions of semiconductor devices to submicrometer scales has encouraged the development of *in-situ* two-dimensional potential profile measurement techniques with high spatial resolution, such as Kelvin probe force microscopy [1], [2]. GaAs HEMT's cross-section [3] and cleaved GaAs/AlGaAs  $n$ - $i$ - $p$ - $i$  structures [4] have been studied. The shrinkage of semiconductor devices dimensions as well as ever more powerful computing capabilities have encouraged the development of two-dimensional (2D) physical model-based simulation tools [5], [6]. We report here the cross-sectional investigation of  $n^+$ -InP/InGaAsP/ $p^+$ -InP PIN laser diodes using KFM and 2D simulations. To our knowledge, this work is the first to investigate electric field and potential distributions in PIN laser diodes using KFM and 2D simulations. 2D simulations are shown to successfully yield an unambiguous interpretation of KFM measurements.

## II. EXPERIMENTAL

The PIN laser diode studied was grown by MOCVD. It consists of four layers: an  $n$ -doped InP substrate ( $N_D \approx 2 \cdot 10^{18} \text{ cm}^{-3}$ ), a 280 nm thick undoped InGaAsP layer followed by a  $p$ -doped 1.7  $\mu\text{m}$ -thick InP layer ( $N_A \approx 1 \cdot 10^{18} \text{ cm}^{-3}$ ) and a  $p^+$ -doped 180 nm-thick InGaAs cap layer.

First we have performed KFM scanning of the surface. The measured potential distribution as well as potential and electric field profiles are shown in Fig. 1. The potential difference between the  $n$ - and  $p$ -doped regions is clearly visible and is equal to 600 mV. Spikes in the electric field profile allow us to very precisely locate the interfaces between the various layers. The spacing between

the two central spikes yields an intrinsic InGaAsP layer thickness of 220 nm, which is 20% lower than the nominal value of 280 nm. The discrepancy can be explained by the fact that the PIN laser was fabricated from a piece laying at the edge of the wafer where the layer thicknesses depart from the nominal values.

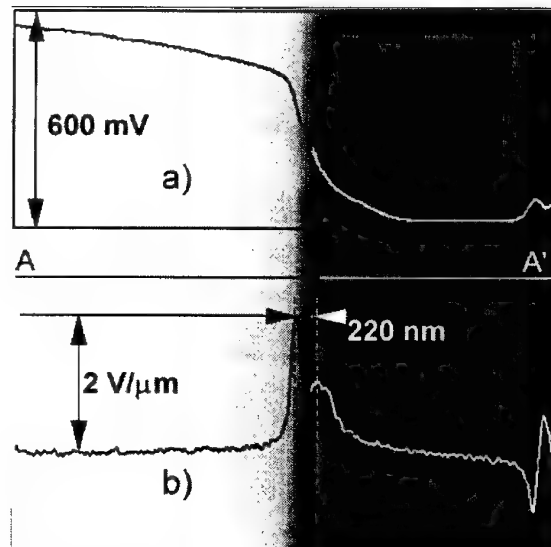


Fig. 1. Measured KFM potential and a) potential and b) electric field profiles along cutline A-A'. Scanned area:  $4 \mu\text{m} \times 4 \mu\text{m}$ .

## III. SIMULATIONS

Simulations were performed using the commercially available package ATLAS/BLAZE from SILVACO, Santa Clara, CA, based on a two-dimensional finite element grid structure. Great care was taken to match the simulated structure to the measured one. We used an energy-balance model taking the non-local phenomena into account to describe carrier transport. For InP, given conduction- and valence-band densities of states  $N_C$  and  $N_V$  of  $5.47 \cdot 10^{17} \text{ cm}^{-3}$  and  $1.15 \cdot 10^{19} \text{ cm}^{-3}$ , respectively, the  $n$ -type InP substrate is degenerated and Fermi-Dirac statistics was used instead of the approximated Boltzmann statistics. Fig. 2 shows the simulated potential along the A-A' cutline before convolution with the KFM tip-transfer function.

The simulated potential difference  $U_c$  between  $n$ - and  $p$ -

doped regions is 1.35V and corresponds to the difference in the work functions for the two materials. It can be approximated to 1.32V using Eq. (1):

$$U_c = \frac{E_g}{q} - \frac{kT}{q} \ln \left( \frac{N_C N_V}{N_A N_D} \right) \quad (1)$$

where  $E_g$  is the InP bandgap and  $N_A$ ,  $N_D$ ,  $N_C$ ,  $N_V$  have been defined before. The slight difference between the simulations and the calculation using (Eq. 1) is due to the degenerated nature of the n-doped substrate for which Fermi-Dirac statistics are required. Fig. 2 also shows the result of the necessary convolution of the simulated potential with the transfer function of the tip as the KFM method is a surface-integration technique and the tip has finite dimensions.

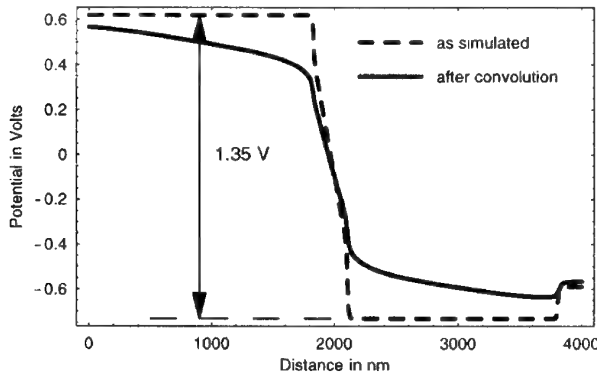


Fig. 2. Simulated potential before and after convolution with the KFM tip transfer function

Measured (Fig. 1) and simulated (Fig. 2) potential are qualitatively very similar. The measured potential is seen to be approximately a factor of 0.4 smaller than the simulated one. Two mechanisms can be put forward to explain this discrepancy: incomplete ionization of the donors and presence of surface states. We therefore implemented these two mechanisms in the simulator. The incomplete ionization mechanism implemented by using Eq. (2):

$$N_D^+ = \frac{N_D}{1 + g_D \exp \left( \frac{E_{F_n} - E_D}{kT} \right)} \quad (2)$$

where  $g_D$  is the degeneracy factor for the conduction band and  $E_{F_n}$  is the quasi-Fermi level for electrons. The incomplete ionization model decreases the voltage difference by about 0.1V. As for the second mechanism, KFM measurements performed in the air always lead to the adsorption of contaminants such as water and the creation of oxides and hydroxides which influence the workfunction of the materials under study. We therefore implemented traps in our simulations (data from Iliadis *et al.* [7]). The simulated structure was divided into three parts (Fig. 3). The bottom part was free of traps, the middle part was with volume traps (concentration as in [7]). To simulate surface states, we implemented donor and acceptor deep traps in the top part of the structure[6].

Fig. 3 shows the simulated potential and the convolute profile for each of the three regions. The deep trap concentration was adjusted in the top part to get a potential profile similar to the KFM profile which yields a trap concentration of approximately  $5 \cdot 10^{19} \text{ cm}^{-3}$ .

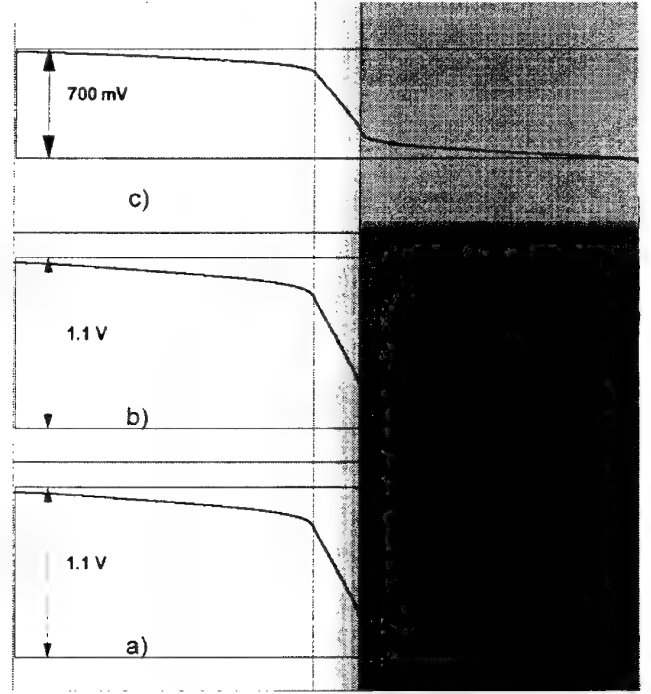


Fig. 3. Simulated potential with incomplete ionization and a) no traps, b) volume traps, c) surface traps. The potential profiles are given after convolution with KFM tip transfer function and the simulated area is  $4 \mu\text{m}$  wide.

#### IV. CONCLUSION

We measured a cross-sectional PIN laser diode potential profile with Kelvin probe force microscopy. 2D simulations showed that the reduced potential drop compared to the theoretical value could be explained in terms of incomplete ionization and surface states. Combined use of KFM and 2D simulations offers new vistas for the characterization of semiconductor devices.

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Thursday, May 27, 1999 10:50 am

# HBTs

- *High efficient AlGaAs/GaAs HBTs for Mobile Communications*

M. Achouche, S. Kraus, S. Hahle, W. John, M. Mai, D. Rentner, T. Spitzbart, P. Wolter,  
H. Wittrich, T. Bergunde, F. Brunner, P. Kurpas, E. Richter, M. Weyers, J. Würfl, G. Tränke  
FBH, Berlin, Germany

p. 101
- *RF power HBTs: modelling and optimization of the electrothermal behavior*

P. Souverain, T. Camps, J. Tasselli, A. Cazarré, A. Marty, and J.P. Bailbé  
LAAS-CNRS, Toulouse, France

p. 103
- *Evidence and characterization of ballistic transport in InP-based HBTs*

D. Sicault, R. Teissier, J-L. Pelouard, F. Pardo, and F. Mollot  
L2M-CNRS, Bagneux, France

p. 105
- *High performance InP based technology for optoelectronic applications*

C. Bergamaschi, A. Huber, D. Huber, V. Schwarz, M. Rohner, T. Morf, and H. Jäckel  
ETH Center, Zürich, Switzerland

p. 107
- *Self-aligned InP/InGaAs double heterojunction bipolar transistors for high  
bit-rate circuit applications*

M. Riet, S. Blayac, J-L. Benchimol, P. André, P. Berdager, A-M. Duchenois, J. Godin.  
OPTO+/CNET, Marcoussis, France

p. 109
- *Size effects in low InP/InGaAs DHBTs*

S. Blayac, M. Riet, J-L. Benchimol, A-M. Duchenois, P. Berdager, J-P. Medus, and J. Godin  
OPTO+/CNET, Marcoussis, France

p. 111
- *High speed collector-up MHBts*

S. Demichel, F. Pardo, R. Teissier, and J-L. Pelouard  
L2M-CNRS, Bagneux, France

p. 113

## High Efficient AlGaAs/GaAs HBTs for Mobile Communications

M. Achouche, S. Kraus, S. Hähle, W. John, M. Mai, D. Rentner, T. Spitzbart, P. Wolter, H. Wittrich, T. Bergunde, F. Brunner, P. Kurpas, E. Richter, M. Weyers, J. Würfl, G. Tränkle

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The rapid development of wireless communication and new services like satcom has created a need for high performance RF components. In this context, power amplifiers based on GaAs-HBTs have received wide acceptance in mobile telephone market because of their remarkable microwave power capabilities and efficiency. In this paper, AlGaAs/GaAs HBTs are developed using production-like processes (i-line stepper, 3" and 4" wafers) for microwave power application. The fabricated sub-cell power HBT with  $3 \times 30 \mu\text{m}^2$  emitter area yield a maximum current gain of 90 with  $f_{\text{max}} > 100 \text{ GHz}$ . Using this technology,  $12 \times 3 \times 30 \mu\text{m}^2$  power cell HBTs exhibit 1 W output power and more than 56% power added efficiency at 3 V operating bias.

The In-house MOCVD-grown AlGaAs/GaAs HBT layer structure is presented in Table 1. The power HBT process uses a double-mesa approach to access the base and collector. Device isolation is ensured by  $\text{He}^+$  ion implantation. The process flow of our L-band HBTs fabrication has been already reported and is mainly based on a selective dry-etching process for emitter mesa realization [1]. Emitter fingers interconnection is made by Ti/Pt/Au metal evaporation or/and  $10 \mu\text{m}$  electroplated gold (thermal shunt). Fig.1 shows SEM pictures of an L-Band power cell HBT. The wafer average DC current gain is 90 with a dispersion of 8 % (this value has been obtained on two different batches of  $5 \times 3$ "). The intrinsic base sheet resistance is  $200 \Omega/\square$  with a dispersion of 7 % over the wafer.

Typical I-V curves for an HBT with an emitter size of  $3 \times 30 \mu\text{m}^2$  (sub-cell) are shown in Fig. 2-a. The power HBT reaches a  $1 \times 10^5 \text{ A/cm}^2$  collector current density level at a  $V_{\text{CE}}$  of 0.6 V, indicating a good collector turn-on characteristic and shows a low off-set voltage of about 0.1 V. All these characteristics are favorable for high efficient devices operating at low bias supply voltage. Fig. 2-b shows RF characteristics of a  $3 \times 30 \mu\text{m}^2$  area HBT at a collector current density of  $J_{\text{CE}} = 3 \times 10^4 \text{ A/cm}^2$ . A  $f_t$  of 33 GHz and a  $f_{\text{max}}$  of 106 GHz are extrapolated. The average  $f_t$  is 32 GHz with a  $f_{\text{max}}$  of 101 GHz. Standard deviations are 2 GHz and 6 GHz, respectively. The small signal gain MUG @ 2 GHz and MAG @ 2 GHz are 33 dB and 26 dB, respectively. This high RF performance is probably associated to improved base-collector capacitance obtained by ion implantation or/and improved emitter inductance with our new air-bridge emitter interconnection technology ( $10 \mu\text{m}$  thick electroplated gold). Small signal gain MAG remains high even at 10 GHz (18.5 dB).

A typical power cell HBT contains several sub-cells in parallel. The objective is to increase the output power of the device without substantial degradation of its reliability and microwave performance, which is sensible to extrinsic elements ( $R_B$ ,  $R_E$ ,  $R_C$  and  $L_E$ ). In addition, to manage the heat generated during power operation, it is important to improve device thermal limitations. Using a thermal shunt technology, power cell HBTs with  $10 \times 3 \times 30 \mu\text{m}^2$  emitter area have a small signal gain MUG @ 2 GHz and MAG @ 2 GHz of 31 and 24 dB, respectively, which constitute a degradation of only 2 dB compared to the sub-cell.

Power measurements were carried out on the wafer at 2 GHz using an active load-pull system for large signal characterization. The input load reflection coefficient is adjusted to reach maximum output power. Fig. 3-a shows the output power  $P_{\text{out}}$  and power added efficiency PAE against input power  $P_{\text{in}}$ , measured at  $V_{\text{CE}}$  of 3 V for a power cell of  $12 \times 3 \times 30 \mu\text{m}^2$  emitter area. The device delivered an output power of 1 W corresponding to a power density of  $2.8 \text{ W/mm}$  with more than 56 % PAE. These data demonstrate, that the developed HBTs have a great potential for wireless mobile PCN applications. The power cell HBTs have also been tested under large signal conditions at a supply voltage  $V_{\text{CE}}$  of 8 V, as shown in Fig. 3-b. 3 W output power is measured (power density of  $8.4 \text{ W/mm}$ ) with more than 70 % power added efficiency. These results shows high power handling capabilities of HBTs also under high bias operations.

[1] M Achouche, S Hähle, P Heymann, W John, S Kraus, M Mai, D Rentner, E Richter, T Spitzbart, P Wolter, H Wittrich, J Würfl, G Tränkle: „AlGaAs/GaAs Heterojunction Bipolar Transistors for L-Band Applications“, WOCSDICE'98 pp.47-48.

| Material        | Doping [ $\text{cm}^{-3}$ ] | Function             |
|-----------------|-----------------------------|----------------------|
| InGaAs          | $1 \times 10^{19}$ (Se)     | Cap                  |
| InGaAs --> GaAs | $1 \times 10^{19}$ (Se)     | Cap grading          |
| GaAs            | $5 \times 10^{18}$ (Si)     | GaAs-cap             |
| GaAs --> AlGaAs | $3 \times 10^{17}$ (Si)     | Emitter grading      |
| AlGaAs          | $3 \times 10^{17}$ (Si)     | Widgap-emitter       |
| AlGaAs --> GaAs | $3 \times 10^{17}$ (Si)     | Emitter-base grading |
| GaAs            | $4 \times 10^{19}$ (C)      | Base                 |
| GaAs            | $2 \times 10^{16}$ (Si)     | Collector            |
| GaAs            | $5 \times 10^{18}$ (Si)     | Subcollector         |

Table1 Epitaxial layer structure of the AlGaAs/GaAs HBTs

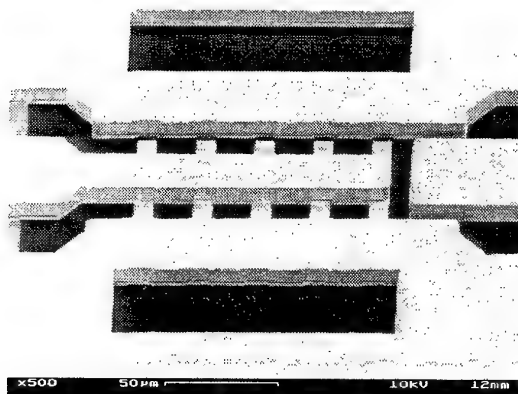
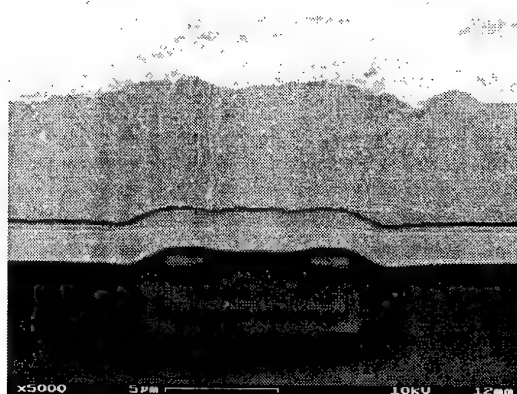
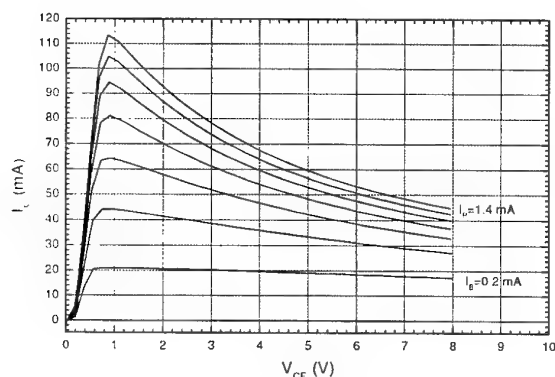
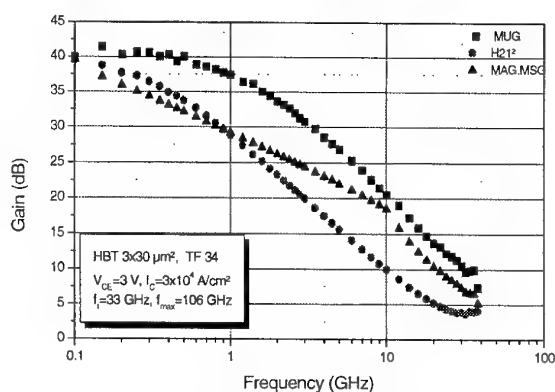
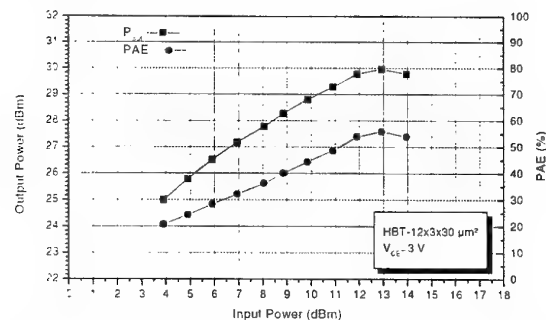
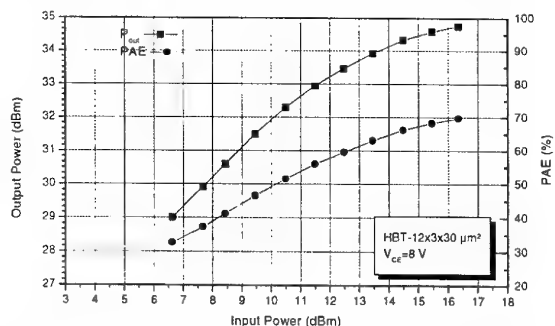
Fig. 1-a Fishbone-type power L-band HBT with 10  $\mu\text{m}$  thermal shunt technology

Fig. 1-b Emitter interconnection using evaporated and electroplated metallization

Fig. 2-a  $I_{CE}$ - $V_{CE}$  characteristics of an AlGaAs/GaAs-HBT ( $3 \times 30 \mu\text{m}^2$ )Fig. 2-b RF characteristics of a  $3 \times 30 \mu\text{m}^2$  AlGaAs-GaAs-HBT ( $J_{CE}=3 \times 10^4 \text{ A/cm}^2$ )Fig. 3-a Output power  $P_{out}$  and power added efficiency PAE against input power  $P_{in}$ , measured at 2 GHz for a  $12 \times 3 \times 30 \mu\text{m}^2$  power HBT ( $V_{CE}=3 \text{ V}$ )Fig. 3-b  $P_{out}$  and power added efficiency PAE against input power  $P_{in}$ , measured at 2 GHz for a  $12 \times 3 \times 30 \mu\text{m}^2$  power HBT ( $V_{CE}=8 \text{ V}$ )

# RF POWER HBTs: MODELLING AND OPTIMISATION OF THE ELECTROTHERMAL BEHAVIOUR

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## 1. Introduction

For high frequency power amplification GaAs heterojunction bipolar transistors (HBT's) exhibit better capabilities than GaAs MESFET's in terms of admissible power densities, high efficiency and linearity. The technological development of the HBT has lead for example to power densities of 50 kW/cm<sup>2</sup> in L and S-bands with power-added efficiency (P.A.E) of 50 % [1,2]. We report in this paper power performances at 1.8 GHz for HBT's fabricated in our laboratory. Experimental results are compared with the simulated ones issued from the large-signal electrothermal modelling that we have developed. On the basis of accurate 3D thermal modelling, we discuss on the opportunity to transfer the transistor active layers onto host substrates of better thermal conductivities such as Diamond or Aluminum Nitride (AlN). The technological solutions investigated are described and the first results obtained on large devices are presented.

## 2. RF Characterization

We have fabricated both GaAlAs/GaAs and GaInP/GaAs HBT's, with epitaxial layers grown respectively by MBE (with a Be-doped base) and by MOCVD (with a C-doped base) [3]. The HBT structure is based on a typical mesa technology with unit emitter area of 6 x 60 µm<sup>2</sup>. As illustrated on figure 1 for a one-emitter finger HBT, a 10 µm-thick emitter air-bridge along the emitter provides an uniform current distribution into the device and a better thermal dissipation. Self-aligned GaInP transistors exhibit a cut-off frequency  $f_T$  of 20 GHz and a maximum oscillation frequency  $f_{max}$  of 40 GHz, for 20 mA collector current and 5 V collector bias. Figure 2 illustrates GaAlAs/GaAs the measured output power ( $P_{out}$ ) and PAE characteristics as a function of the input power ( $P_{in}$ ) at 1.8 GHz in class AB operation. The output power is 27 dBm (500 mW) at a collector voltage of 8 V with an associated PAE of 60 %, corresponding to a RF power density of 150 kW/cm<sup>2</sup>. These results show the potentialities of HBT devices for wireless applications.

## 3. Thermal analysis of the HBT RF behavior

Many works were focused on recent years on the electro-thermal modeling of the HBT for power applications [5,6]. The large signal electro-thermal model that we have developed is based on the

conventional Gummel-Poon approach with a temperature dependence of all the physical parameters (saturation currents, base transit time,...). Thermal effects are accounted by including a thermal cell consisting of a thermal resistance  $R_{TH}$  and a thermal capacitance  $C_{TH}$  [3]. This model is implemented into the harmonic balance HP-MDS and into SABER simulators.

A 3D modeling of the heat dissipation was also performed with the F.E.M simulator software ABAQUS [7] and taking into account the variation of the thermal conductivity with the temperature. These simulations quantify the decrease of the thermal resistance ' $R_{TH}$ ' due to the conductive dissipation by the air-bridges through the substrate. The thermal resistance of our device varies as a linear function of the dissipated power  $P_{dc}$ :

$$R_{TH} (^\circ\text{C/W}) = 264 + 70 \times P_{dc}$$

The electrothermal model is then employed to determine the influence of  $R_{TH}$  on the RF power behavior of the transistor. For example, we have analyzed on figure 3 PAE at 2 GHz for two typical  $R_{TH}$  values corresponding to GaAs and AlN substrates. The predicted maximum PAE value at an RF output power of 25 dBm (0.32W) is increased to 55% at around 70% for an identical transistor which active layers would be transferred onto a Diamond carrier. According to the temperature evolution with  $P_{out}$  for different GaAs and diamond thermal resistance, at the compression point, a lower temperature correlated with a 50 % gain of output RF power are predicted (Figure 4). This result is important for reliability considerations.

## 4. Technological solutions

In our Laboratory we investigate a technological method that consists of bonding an HBT inverted epitaxial structure (collector on top) on Diamond or AlN carriers. A low temperature brazing process is performed (~200 °C) by liquid-solid inter-diffusion of the In-Au metallurgical system. The original substrate is then removed by both mechanical and chemical lapping. HBT layers bonding on AlN has been realized showing the feasibility of the different technological steps ( Figure 5.a). The fabricated transistors are of large dimensions (100 x 100 µm<sup>2</sup>): the measured ( $I_C, V_{CE}$ ) characteristics are comparable to those obtained from conventional devices ( Figure 5.b). However, accounting for the large dimensions, we cannot highlight the improvement of power performances.

## 5. Conclusions

High power RF characterization at 1.8 GHz have been reported for a  $6 \times 60 \mu\text{m}^2$  AlGaAs/GaAs HBT in class AB operation. A maximum output power density of  $150 \text{ kW/cm}^2$  was achieved with a 60% power added efficiency. The analysis of heat dissipation has highlighted the advantages of transferring the HBT active layers onto better thermal carriers such as Diamond or AlN. Concerning the experimental part, we have performed HBT's brazing by In-Au liquid-solid inter-diffusion onto AlN: the first results are encouraging and validate this technique.

## 6. References

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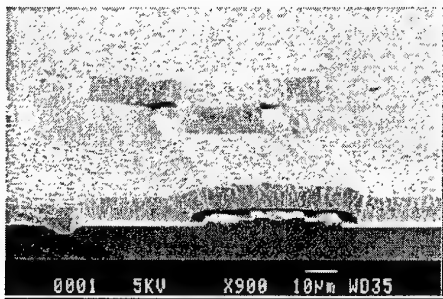


Figure 1: MEB view of a  $6 \times 60 \mu\text{m}^2$  HBT

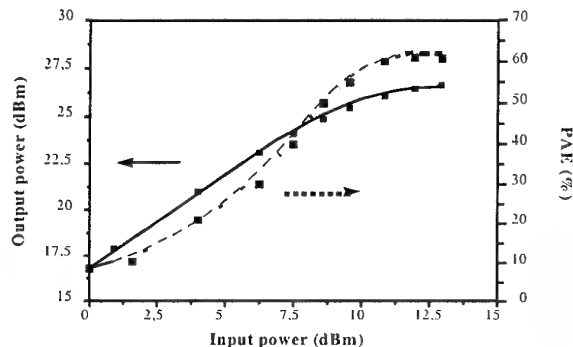


Figure 2: Measured and simulated output power and PAE at 1.8 GHz

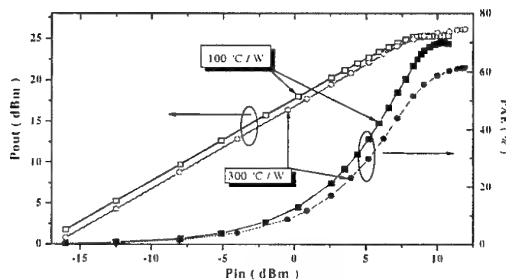


Figure 3: Output power & P.A.E versus input power for GaAs and AlN

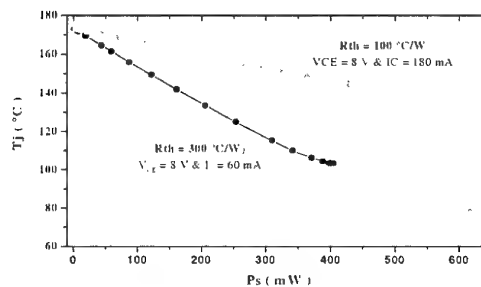


Figure 4: Temperature versus output power for GaAs and AlN

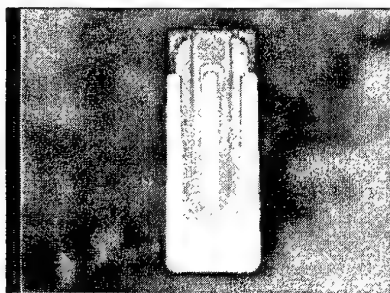


Figure 5.a: Reported HBT after processing

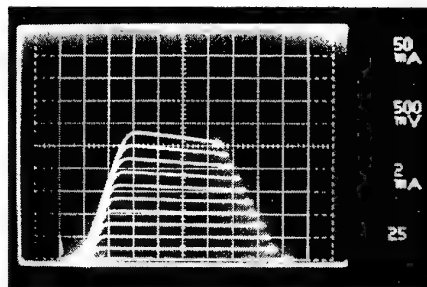


Figure 5.b: Characteristics of an HBT transferred on AlN

## Evidence and characterization of ballistic transport in InP-based HBTs

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In the recent years, InP-based heterojunction bipolar transistors (InP HBT) have demonstrated very impressive high frequency performances ( $f_T$  and  $f_{max} > 200$  GHz). As a matter of fact, total transit times in the devices enter the sub-picosecond domain, making important every improvement of the transport times, as small as 100 fs. In this context, the benefit of non stationary and especially ballistic transport in the base of InP HBTs is of crucial interest.

We have recently reported on the experimental evidence of ballistic transport in the base of InP HBTs, using hot carriers electroluminescence spectroscopy [1]. Ballistic electron injection occurs at the InP/InGaAs emitter-base heterojunction, due to the abrupt conduction band discontinuity. Our EL technique consists in the spectral analysis of the light emitted by the fraction of these hot electrons which recombine with holes in the base, photon energy being directly related to the electron energy (fig. 1). This allowed the ballistic electron distribution to be measured and studied from low temperature to room temperature operating conditions (fig. 2). We also demonstrated that the ballistic electron mean free path could be deduced from the EL signal dependence with base width.

We present here the results of an improved method for measuring ballistic electron mean free path in HBT's InGaAs bases. We recorded EL signal emitted from a large number of emitter-base diodes made of a collector-up HBT structure, for which the base layer was selectively etched down to carefully controlled width. Non-diffusive Ti/Au base contacts were deposited on the top of the bases, and the emitted light was collected through the InP substrate. The absolute EL intensity ( $I_{bal}$ ) originating from the purely ballistic electron population was then obtained as a function of the base width  $W$ . This signal depends on the spatial distribution of ballistic electrons, but also on the efficiency of light emission (fig. 3). Taking into account internal optical interferences due to the reflection of the EL light on the base contact which acts as a mirror, we demonstrated that the  $I_{bal}(W)$  curve modulation pattern (fig. 4) is directly related to the spatial extent of the ballistic population, i.e. to the ballistic electron inelastic mean free path ( $L_b$ ) [2].

This technique permits  $L_b$  to be precisely measured for a large variety of structures or experimental conditions. Figure 5 presents the low temperature dependence of  $L_b$  on base p-doping level ( $N_A$ ), in the range  $3 \cdot 10^{17} \text{ cm}^{-3}$  to  $5 \cdot 10^{19} \text{ cm}^{-3}$ . The ballistic electron energy (150 to 200 meV above the conduction band) corresponds to a forward velocity of about  $10^8 \text{ cm/s}$ . Thus, the measurement of  $L_b$  is equivalent to a measurement of ballistic electron inelastic scattering times (right hand scale on fig. 5). The value of 120 fs obtained for  $N_A = 3 \cdot 10^{17} \text{ cm}^{-3}$  is consistent with a relaxation dominated by LO phonon emission. When  $N_A$  increases, electron-hole interactions become dominant through the emission of LO phonon-hole plasmon coupled modes, leading to scattering times as small as 20 fs. The most remarkable feature is however the rising of  $L_b$  for the larger doping levels ( $N_A > 2 \cdot 10^{19} \text{ cm}^{-3}$ ). This can be explained by a reduction of coupling strength when plasmon energy (varying as  $N_A^{1/2}$ ) becomes much larger than LO phonon energy. In addition, as the energy lost in one scattering event increases, the available final density of states for electron scattering becomes smaller, further reducing scattering efficiency.

The measurement of  $L_b$ , more easily performed at low temperature. Nevertheless, it can be carried out up to room temperature, provided we take into account the overlap of thermalized, quasi-ballistic and ballistic populations. Figure 6 shows that  $L_b$  does not depend much on temperature for  $N_A = 8 \cdot 10^{18} \text{ cm}^{-3}$ . As a matter of fact, hot electron relaxation is dominated by the emission of hole plasmon excitations which, for degenerated hole gas, very little depend on temperature.

We can then conclude that room temperature ballistic electron mean free path also increases for  $N_A > 2 \cdot 10^{19} \text{ cm}^{-3}$  up to a value of about 40 nm for  $N_A = 5 \cdot 10^{19} \text{ cm}^{-3}$ . This indicates that dominant ballistic transport, corresponding to base transit time as fast as 40 fs, is accessible with state of the art HBT technology (base width of 40 nm,  $N_A > 5 \cdot 10^{19} \text{ cm}^{-3}$ ).

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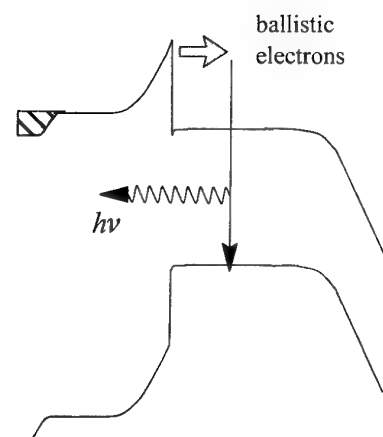


Fig. 1: Emitted photon energy reflects hot electron energy

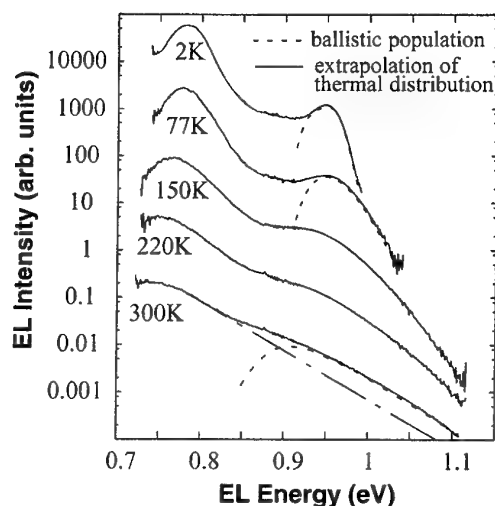


Fig. 2: EL spectra showing ballistic electron populations

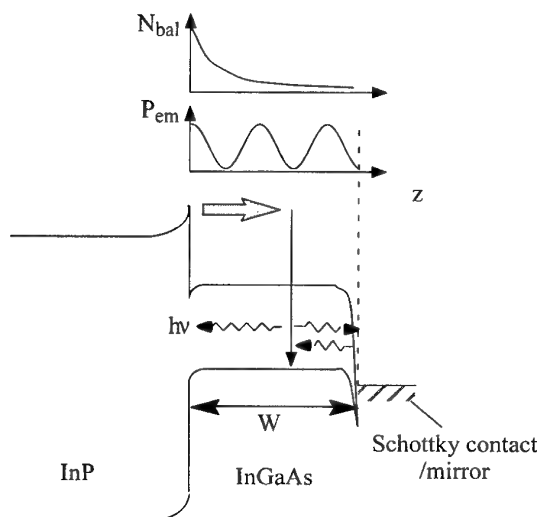


Fig. 3: EL intensity emitted by a diode with base width  $W$ , is the convolution of ballistic electron distribution  $N_{bal}$  and photon emission probability  $P_{em}$ , integrated over the total base width

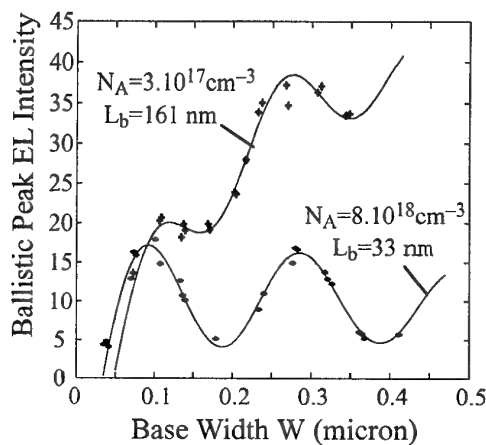


Fig. 4:  $I_{bal}(W)$  curves allowing ballistic electron mean free path to be determined

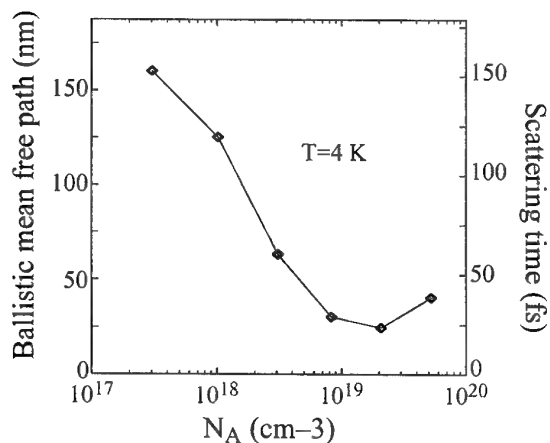


Fig. 5: Evolution of ballistic electron mean free path with base doping level

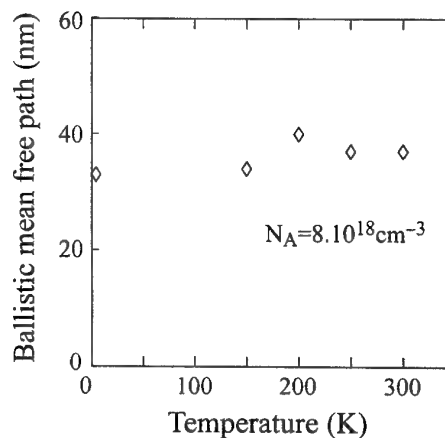


Fig. 6: Evolution of ballistic electron mean free path with temperature

# High Performance InP based HBT Technology for Optoelectronic Applications

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## Abstract

*The authors reports on optimisation and characterisation of InP/InGaAs HBTs, MIM capacitors and planar inductors. These components were used in high performance optoelectronic applications.*

## Device Technology:

The InP/InGaAs HBT is based on a MOCVD-grown single hetero epitaxial layer structure. To improve the high speed performance the base and collector thickness were reduced to 50 nm and 400 nm respectively. [1]

After optical lithography, a wet etching process step is used for the formation of the emitter mesa resulting in an undercut which enables self aligned emitter and base contacts. (Fig. 1) The minimum emitter size is  $0.5\mu\text{m} \times 3\mu\text{m}$ .

The resistors are made of evaporated Cr-Films having a sheet resistance of  $50\Omega/\text{square}$ . The capacitors have a MIM structure with  $\text{Ta}_2\text{O}_5$  as dielectric and a typical capacitance per area of  $0.6\text{fF}/\mu\text{m}^2$ . Using an optimised layout the series resistance of the capacitance were minimised.

## Characterisation:

The HBTs achieve a DC current gain of 25 (Fig. 2). The values of  $f_T$  and  $f_{\text{max}}$  were extrapolated from on-wafer S-parameter measurements up to 120GHz. At a collector current density of  $1.3\text{ mA}/\mu\text{m}^2$  and a collector-emitter voltage of 2V,  $f_T$  and  $f_{\text{max}}$  reach 130 GHz and 220 GHz respectively for a  $1\mu\text{m} \times 8\mu\text{m}$  device.

A complete low frequency (0.2 Hz to 500 kHz) and high frequency (2 to 26 GHz) noise characterisation as a function of emitter-geometry, temperature, and bias-point was carried out [2]. (Fig. 3) For the design an elaborated small signal and noise model is used.

## Circuits

Using these components key building blocks for a 40Gbit/s transmission system have been realized. Results of the 46 GHz monolithically integrated Photoreceiver [1] and the 50 GHz HBT amplifier [3] will be presented.

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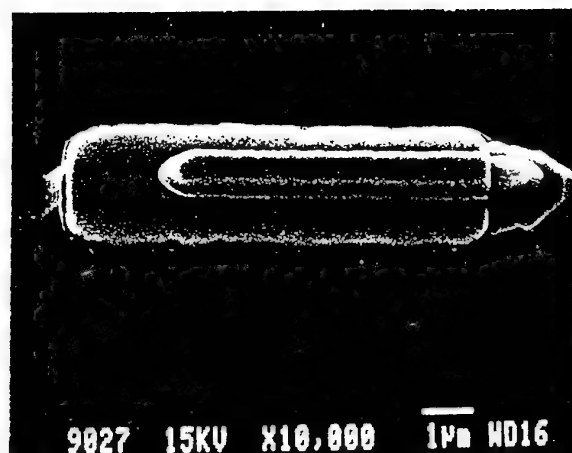
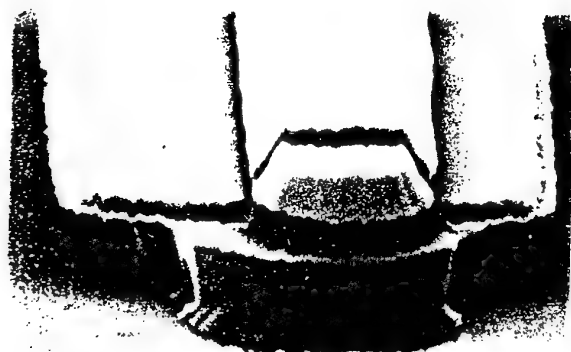


Figure 1 SEM Pictures of a InP/InGaAs HBT with an emitter area of  $1\mu\text{m} \times 5\mu\text{m}$

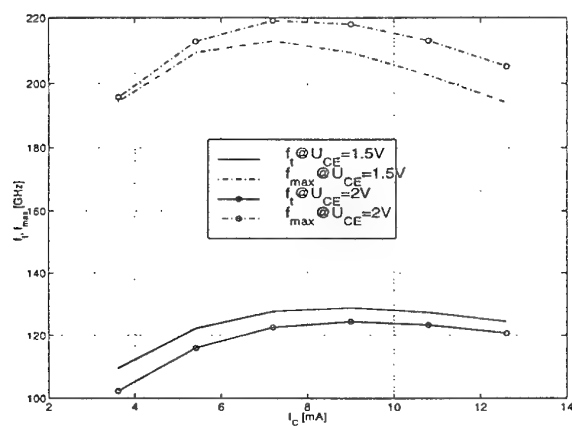


Figure 2 a)  $f_T$  and  $f_{\max}$  vs collector current  
 $A_E = 1 \times 8 \mu\text{m}^2$

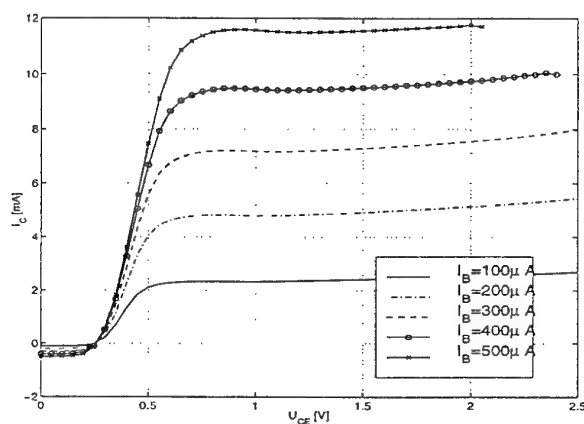


Figure 2 b) Measured  $I_C$  vs  $U_{CE}$  characteristic  
 $A_E = 1 \times 8 \mu\text{m}^2$

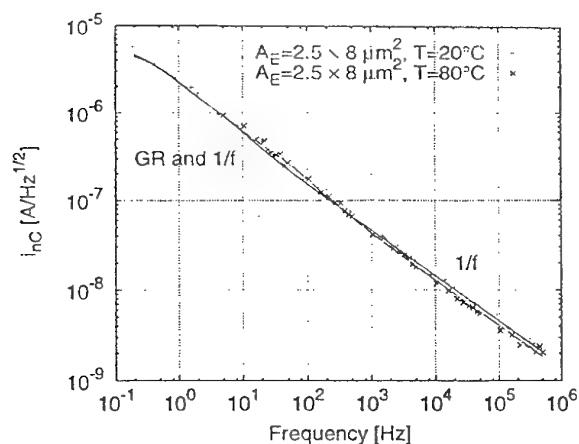


Figure 3 a)  
Measured (symbols) and simulated (-) collector current noise spectral density at the collector  
 $I_C = 8 \text{ mA}$   
 $A_E = 2.5\mu\text{m} \times 8\mu\text{m}$  and  $A_E = 1.5\mu\text{m} \times 8\mu\text{m}$

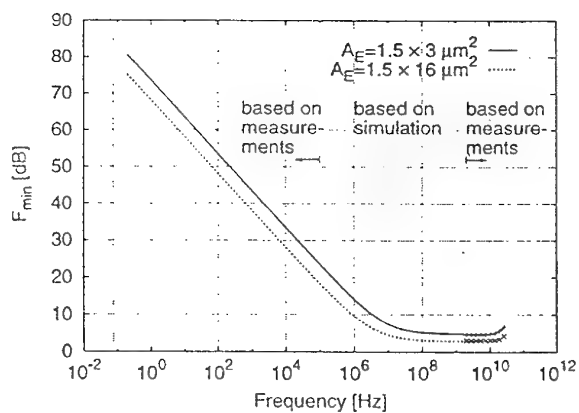


Figure 3 b)  
Simulated minimum noise figure  $F_{\min}$   
 $A_E = 1.5\mu\text{m} \times 3\mu\text{m}$  and  $A_E = 1.5\mu\text{m} \times 16\mu\text{m}$

## Self-aligned InP/InGaAs Double-Heterojunction Bipolar Transistors for High Bit-Rate Circuit Applications

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**Introduction:** InP-based Heterojunction Bipolar Transistors (HBTs) have shown great potential in high-speed electronics due to their excellent high-frequency characteristics [1]. This paper describes an InP/InGaAs DHBT technology for 40 Gb/s IC's. For these circuit applications [2, 3], sufficient breakdown voltage ( $>5$  V), static gain around 50, cut-off frequencies ( $f_T$ ) and maximum oscillation frequencies ( $f_{max}$ ) greater than 100 GHz are needed. High performance InP/InGaAs DHBTs grown by chemical beam epitaxy deposition (CBE) are reported with a  $f_T$  of 168 GHz and  $f_{max}$  of 137 GHz at a current density of  $1 \text{ mA}/\mu\text{m}^2$ . The devices have  $51 \mu\text{m}^2$  total emitter area and exhibit current gain equal to 50. Their breakdown voltage is 6 V. The three main optimizations concern the base epitaxial layer (doping level, thickness and composition), the reduction of the collector thickness and the reduction of the base-collector active area.

**DHBT epitaxial structure:** The epitaxial layer structure (Tab. 1), grown by CBE deposition, consists of (from bottom to top) a  $4000\text{\AA}$  N+ InP sub-collector, a N+ InGaAs collector contact layer, a N+ InP layer, a  $2000\text{\AA}$  undoped InP collector layer, a  $400\text{\AA}$  N InGaAsP layer, a  $400\text{\AA}$  undoped InGaAs spacer, a  $550\text{\AA}$  P+ InGaAs graded base, a  $1500\text{\AA}$  N InP emitter, a N+ InP layer, and a N+ InGaAs emitter cap. A carbon doped graded base ( $\text{Ga}_{1-x}\text{In}_x\text{As}$  with  $0.46 < x < 0.53$ ) permits to increase the electric field in the base and to obtain a sufficient current gain with relatively high base doping level and thickness. A  $2000\text{\AA}$  InP collector thickness is a good trade-off to obtain a minimum transit time in the collector together with a still acceptable base-collector capacitance.

**DHBT technology:** To reduce base-collector area and base resistance (Fig. 1), self-aligned HBTs are fabricated using selective wet chemical etchants and dry etching process [4]. First, the TiAu emitter contact is lift-off from the InGaAs cap layer; this metal is used as a mask for the emitter mesa wet etching. The etchants are  $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  and  $\text{H}_3\text{PO}_4:\text{HCl}$  for the InGaAs and the InP layers. The wet etching forms a slight undercut around the emitter contact. Base metal of TiAu is evaporated over the region including the emitter mesa. Next, the base mesa etching is performed; the mesa is defined by the base metal with a combination of ion beam etching and wet chemical etching. An undercut is formed in the collector layer to reduce the base-collector junction area. Next, a self-aligned TiAu collector contact is evaporated. Then, the collector mesa is performed by a wet chemical etching to isolate the devices (Fig. 2). A polyimide film is used for passivation and planarization. Finally, TiAu metal is used to connect devices to external pads.

**Results and discussion:** The common-emitter I-V characteristics of a typical  $51 \mu\text{m}^2$  InP/InGaAs HBT are shown in Fig. 3. The collector-emitter offset voltage is 200 mV; Gummel plot measured at 0 V base-collector voltage indicate that ideality factors are respectively 1.1 and 1.2 for the E-B and B-C junctions. The collector-emitter breakdown voltage  $\text{BV}_{\text{CEO}}$  is 6 V at  $50 \mu\text{A}$ .

On-wafer S-parameter measurements up to 40 GHz were performed. The measurements are carried out at a collector-emitter bias voltage  $V_{\text{CE}}$  of 1.6 V. The highest values for  $f_T$  and  $f_{max}$  (Mason's gain) are 168 GHz and 137 GHz respectively at collector current density  $J_C$  of  $1 \text{ mA}/\mu\text{m}^2$  (Fig. 4). This corresponds to an effective  $R_{\text{B}}C_{\text{BC}} = f_T / (8\pi f_{\text{max}}^2)$  delay time of 0.38 ps. The relatively small  $R_{\text{B}}C_{\text{BC}}$  is a result of the low base-collector capacitance.

Circuits operating up to 50 Gb/s, such as a selector, have been fabricated with those transistors [5].

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Table 1 : Layer structure of the InP/InGaAs DHBT

| Layer        | Material  | Thickness (nm) | Doping (cm <sup>-3</sup> ) |
|--------------|-----------|----------------|----------------------------|
| Emitter cap  | n+ InGaAs |                | $1.5 \times 10^{19}$       |
|              | n+ InP    |                | $1.5 \times 10^{19}$       |
| Emitter      | n InP     | 150            | $2 \times 10^{17}$         |
| Base         | p+ InGaAs | 55             | $4 \times 10^{19}$         |
|              | InGaAs    | 40             | Undoped                    |
| Collector    | InGaAsP   | 40             | $1 \times 10^{17}$         |
|              | InP       | 200            | $1 \times 10^{16}$         |
|              | n+ InP    |                | $1.5 \times 10^{19}$       |
| Subcollector | n+ InGaAs |                | $1.5 \times 10^{19}$       |
|              | n+ InP    |                | $1.5 \times 10^{19}$       |

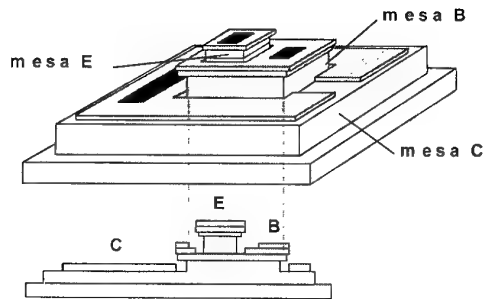


Fig. 1. Schematic structure of self-aligned InP/InGaAs DHBT.

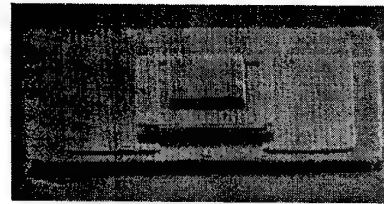
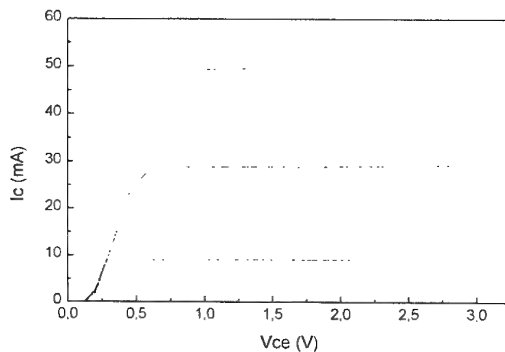
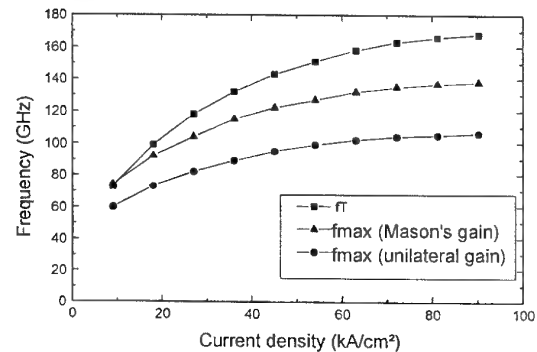


Fig. 2. Scanning electron micrograph of self-aligned InP/InGaAs DHBT.

Fig. 3. Common-emitter current-voltage characteristics of a  $2.6 \times 19.6 \mu\text{m}^2$  DHBT.Fig. 4. Dependence of  $f_T$  and  $f_{\text{max}}$  on collector current density for a  $2.6 \times 19.6 \mu\text{m}^2$  DHBT

## Size effects in low power InP/InGaAs DHBTs

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**Introduction:** Low consumption high speed ICs require low power transistors with sufficient dynamic performances[1]. InP/InGaAs system exhibits low turn-on voltage and low surface recombination velocity. This material is thus particularly well-suited for the fabrication of small emitter HBTs without important current gain degradation [2]. DHBTs with 2.6 $\mu$ m emitter width and length ranging from 2.6 to 19.6  $\mu$ m are presented. The smallest transistor exhibits  $f_t/f_{max}$  of 84/104GHz at  $I_c=2$ mA, maximum performance of 110/138GHz at  $I_c=5$ mA and current gain=50. Effects of device scaling on the current gain and the RF performances are studied here.

**Device structure and fabrication process:** InP/InGaAs double heterojunction bipolar transistors are grown using chemical beam epitaxy. The device structure includes a compositionally graded base allowing simultaneous high base doping for low base resistance and sufficient current gain [3]. A step graded collector using InGaAsP alloy minimizes the current-blocking effect at the base-collector junction. The transistors are fabricated with E/B and B/C self-alignment process [4] using undercuts obtained by wet side-etching. A large collector undercut allows minimization of the base collector capacitance.

**Device results:** The common emitter static characteristic of the 2.6 $\times$ 2.6 $\mu$ m<sup>2</sup> DHBT is shown in figure 1. The collector-emitter offset voltage is 180mV. A plot of the small signal current gain as a function of the collector current for the different emitter lengths is shown in figure 2. No emitter-size effect can be seen on this parameter, this is attributed to the low recombination velocity of InP and to the graded base. S-parameters measurements are carried out at  $V_{ce}=1.6$ V. Figure 3 shows the obtained values of  $f_t$  (unity current gain) and  $f_{max}$  (unity Mason's gain) as a function of the collector current.  $f_t/f_{max}$  of 84/104GHz at  $I_c=2$ mA, and 110/138 GHz at 5 mA are obtained on the 2.6 $\times$ 2.6 $\mu$ m<sup>2</sup> device. The 9.6 $\times$ 2.6 $\mu$ m<sup>2</sup> exhibits  $f_t/f_{max}$  of 159/154 GHz at  $I_c=30$ mA. As expected, the best performances at low collector current are obtained on small emitter transistors. However the maximum  $f_t$  value decreases with the emitter length. Best  $f_{max}/f_t$  ratios are obtained for small transistors since the  $R_b \times C_{bc}$  product depends on the intrinsic value of the collector-base capacitance which is proportional to the emitter area. A plot of the different contributions to total delay time ( $1/(2\pi f_t)$ ) is shown in figure 4. Total transit time ( $\tau_f$ ) is independent on emitter size. For the 15 and 20 $\mu$ m emitter long transistors, transit time and collector charging time ( $\tau_{cc}$ ) are balanced. As the emitter length gets smaller,  $\tau_{cc}$  increases regularly and is responsible for the fall of  $f_t$ .

**Discussion:** At high current densities, the emitter-base dynamic resistance value and its associated time constant are low. All the other terms of the total delay time are independent on the geometry, except the product of static emitter resistance by base-collector capacitance ( $R_e \times C_{bc}$ ). This term takes part of collector charging time and is proportional to collector to emitter area ratio ( $S_c/S_e$ ). Clear correlation between this ratio and the collector charging time can be observed in figure 5. The plot of  $C_{bc}$  as a function of  $I_c$  for the different emitter lengths clearly indicates that this capacitance is not proportional to the emitter area (fig. 6). This is explained by the fact that an excess base collector area is required for base interconnection and that its proportion over the whole base-collector area becomes important for small lengths, resulting in the increase of  $S_c/S_e$  and therefore  $R_e \times C_{bc}$  time constant.

**Conclusion:** InP/InGaAs DHBTs showing good low power operation capabilities were fabricated and characterized. No emitter size effect was found on the small-signal current-gain. The collector to emitter area ratio was found to be the most important factor to be optimized to obtain high frequency performance at low collector current. The base collector area associated to the base pad is thus the main limiting factor of small emitter area devices.

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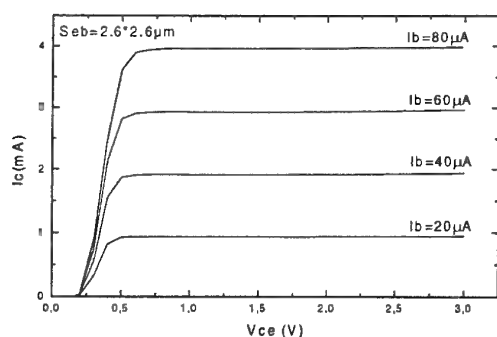
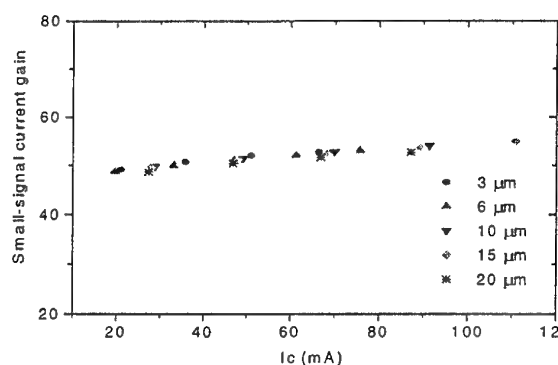
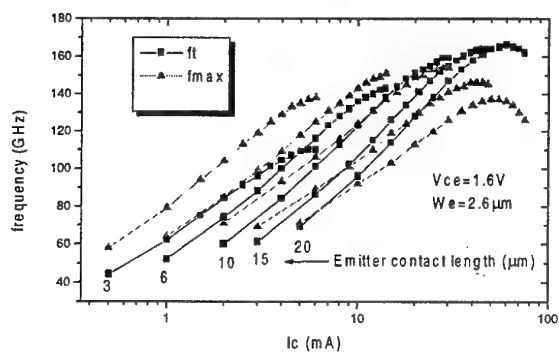
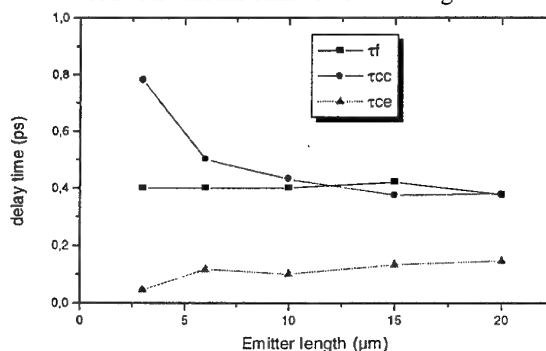
Fig. 1:  $I_c(V_{ce})$  characteristic for a  $2.6 \times 2.6 \mu\text{m}^2$  deviceFig. 2: Plot of the small-signal current gain as a function of  $I_c$  for various emitter contact lengthsFig. 3:  $F_t$  and  $F_{max}(I_c)$  as a function of the collector current for different emitter lengths

Fig. 4: Contributions to the total delay time as a function of the emitter length

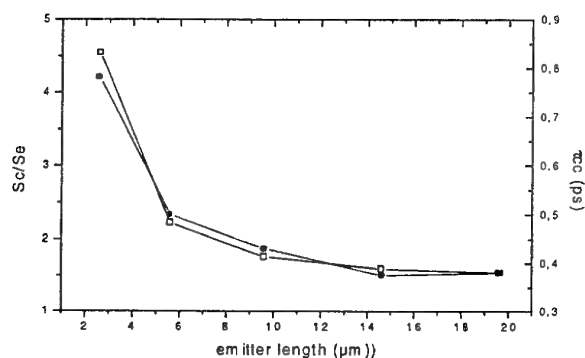
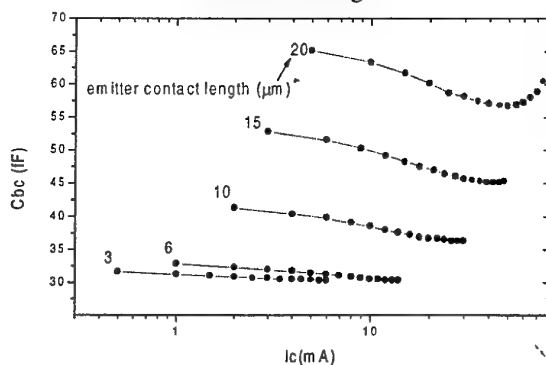


Fig. 5: Correlation between the collector charging time and the collector to emitter area ratio as a function of the emitter length

Fig. 6: Plot of the base collector capacitance as a function of  $I_c$  for various emitter lengths

# High speed collector-up MHBTS

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## Introduction

Advances in technology for heterojunction bipolar transistors (HBTs) are necessary to further improve their performance which are commonly measured in terms of current gain ( $f_T$ ) and power-gain ( $f_{max}$ ) cutoff frequencies. The Metal Heterojunction Bipolar Transistor (MHBT) has already demonstrated a large potential for ultra high speed behavior [1,2]. The Schottky collector is used to reduce both the transit time and the charging time in the base-collector transition layer. Based on a fully self-aligned collector-up process, the MHBT (Fig. 1) fabrication reduces dramatically device parasitics[2] and allows the emitter and collector width to be reduced below submicron dimensions. The full transistor (except pad connections) was patterned with only one photo-lithographic step using selective wet etching and undercut-based processing. In these conditions the base access zone is as short as 0.2  $\mu\text{m}$ .

In order to have a good mechanical resistance after the undercut in the InP emitter layer, the extrinsic part of the base (figure 1) has to be thick enough ( $>0.1\mu\text{m}$ ). In opposition the electron transport through the intrinsic base requires a thin base layer (typically less than 0.05  $\mu\text{m}$ ) for both the current gain and the dynamic behavior. In this paper, we present a new HBT structure which allows to process ultra-thin base MHBT[1] (here  $W_b=0.04\mu\text{m}$ ).

## Novel MHBT structure

This novel MHBT structure is based on a composite base layer which allows to reduce the base transit time keeping a thick extrinsic base layer. A p-type InGaAsP layer is introduced (Fig. 2a) between the InGaAs layer (the heavily doped base layer) and the InP layer (the emitter layer), creating two launching areas for ballistic electrons (Fig. 2b). At the InP/InGaAsP interface, the ballistic population is generated with an excess kinetic energy of 0.1 eV. Because of the low doping level in the quaternary layer ( $10^{18}\text{ cm}^{-3}$ ) electron transport is mainly ballistic and quasi-ballistic through this layer[3]. Then, the electron are re-launched by the InGaAsP/InGaAs interface in the InGaAs base layer which is thin enough to conserve the ballistic behavior[3] despite its high doping level ( $4.10^{19}\text{ cm}^{-3}$ ). Furthermore, the base contacts are directly deposited on the heavily doped layer. Thus non-alloyed contacts (Pt/Ti/Pt/Au) exhibiting low resistivity ( $<10^{-6}\Omega\cdot\text{cm}^2$ ) are used.

## Electric characterizations

The Fig. 3 shows the Gummel plot of a typical  $1\times 36\mu\text{m}^2$  MHBT. The ideality factor of the collector current which is very close to unity ( $n_c=1.02$ ), demonstrate the excellent injection conditions at the InP/InGaAsP abrupt heterojunction. The DC current gain is proportional to  $I_c^{0.21}$  and reaches 20 for the highest current densities.

Microwave performance was evaluated by the measurement of small-signal S parameters from 0.5 GHz to 50 GHz. The typical dynamical behavior for the device is shown on Fig. 4. We can notice that both the current gain and the Mason's invariant power gain exhibit a decrease with frequency of 14 and 15 dB/decade respectively. These low values have already been observed in MHBT structures[2]. Using these slopes for the extrapolation, we found  $f_T=96\text{GHz}$  and  $f_{max}=236\text{GHz}$  at  $V_{CE}=1.4\text{V}$  and  $J_c=230\text{kA/cm}^2$ . Obviously the conventional 20 dB/decade observed on this devices at low current density does not make sense at high density current. Complementary studies are in progress to understand this unusual but reproducible result.

## Conclusion

A new HBT structure has been presented. It allows the fabrication of thin base MHBTs where the base transit time is reduced by a two-launching process for the electron ballistic transport in the base despite the total thickness of the base. Excellent static behavior has been shown. The unusual dynamical behavior needs to be explained.

The authors would especially like to thank Christophe Dupuis for its technical support. Thanks are also due to J.P. Medus for the S-parameter measurements.

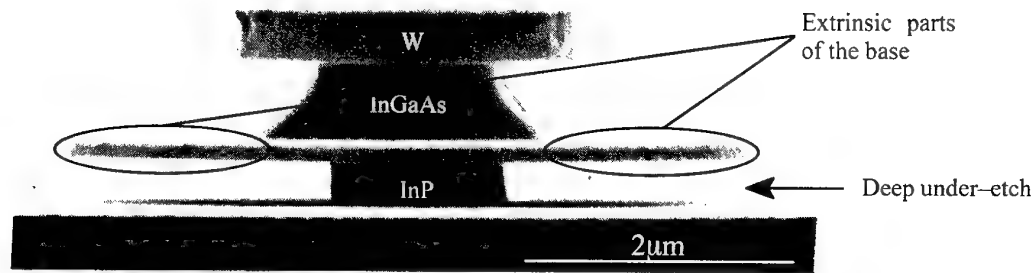
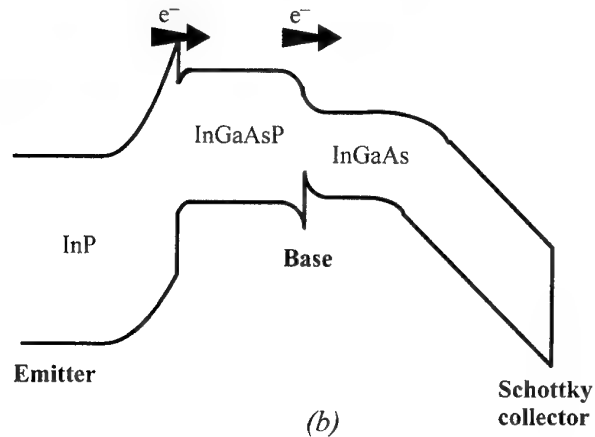


Fig. 1 : SEM view of collector-up HBT.

|   |
|---|
| InGaAs:Si 300nm $5.10^{16}\text{cm}^{-3}$ |
| InGaAs:Be 40nm $4.10^{19}\text{cm}^{-3}$  |
| InGaAsP:Be 80nm $10^{18}\text{cm}^{-3}$   |
| InP:Si 50nm $3.10^{17}\text{cm}^{-3}$     |
| InP:Si 300nm $10^{19}\text{cm}^{-3}$      |
| InGaAs:Si 200nm $10^{19}\text{cm}^{-3}$   |
| S.I. InP                                  |

(a)



(b)

Fig. 2 : (a) GSMBE layer structure and (b) schematic band diagram.

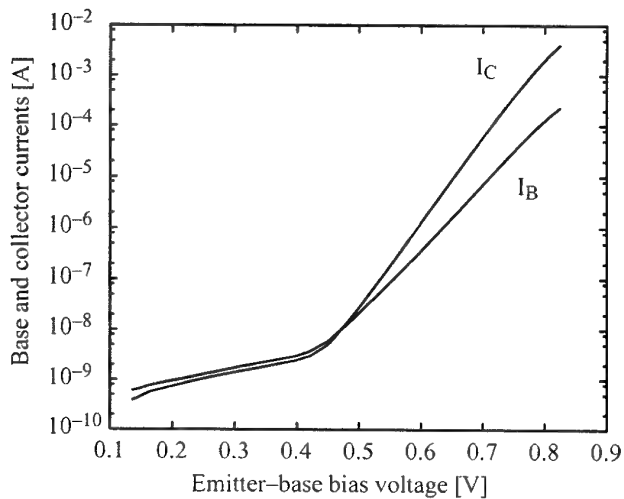


Fig. 3 : Base and collector currents from Gummel plots for  $1 \times 36 \mu\text{m}^2$  emitter size MHBT.

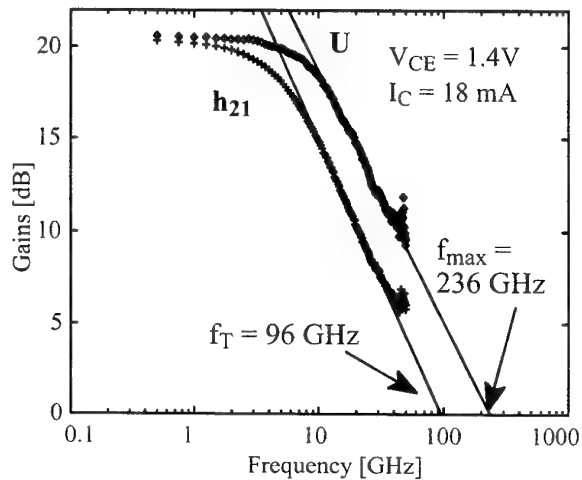
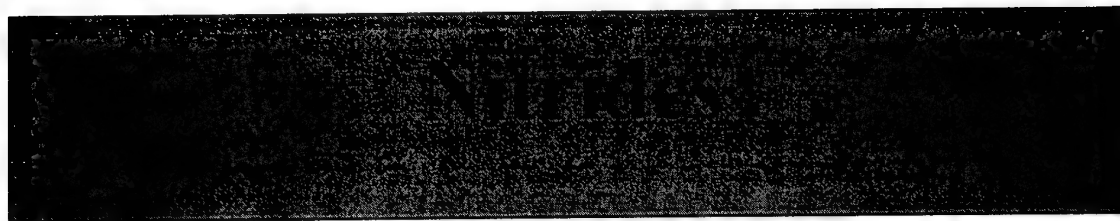


Fig. 4 : The current gain  $|h_{21}|$  and unilateral gain  $U$  as a function of frequency.

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**Friday, May 27, 1999 09:00 am**



- *Group III-Nitride semiconductor transistors for power amplifiers (invited paper)* p. 117  
 John C. Zolper  
 Office of Naval Research, Arlington, VA USA
- *MOCVD grown AlN/GaN HFETs* p. 121  
 E. Alekseev, A. Eisenbach, and D. Pavlidis  
 University of Michigan, Ann Arbor, MI USA
- *Single and double barrier AlGaIn/GaN modulation doped field effect transistors grown by RF assisted MBE* p. 123  
 A. Vescan, A. Wieszt, R. Dietrich, H. Leier, N. Käß<sup>(1)</sup>, E. Kohn<sup>(1)</sup>, J.M. Van Hove<sup>(2)</sup>, P.P. Chow<sup>(2)</sup>, and A.M. Wowchak<sup>(2)</sup>  
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<sup>(1)</sup> University of Ulm, Ulm, Germany  
<sup>(2)</sup> SVT Associates, Eden Prairie, MN USA
- *GaN Static Induction Transistor Fabrication* p. 125  
 N.G. Weimann and L.F. Eastman  
 Cornell University, Ithaca, NY USA
- *GaN MESFETs for high temperature applications* p. 127  
 S. Trassaert, B. Boudart, C. Gaquière, D. Théron, Y. Crosnier, F. Huet<sup>(1)</sup>, M.A. Poisson<sup>(1)</sup>  
 University of Lille-IEMN, Villeneuve d'Ascq, France  
<sup>(1)</sup> Thomson CSF-LCR, Orsay, France
- *Power performance of AlGaIn/GaN HEMTs with 0.2 to 1 mm gate widths* p. 129  
 E. Alekseev, D. Pavlidis, N.X. Nguyen<sup>(1)</sup>, C. Nguyen<sup>(1)</sup>, and D.E. Grider<sup>(1)</sup>  
 University of Michigan, Ann Arbor, MN USA  
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- *How to explain the high breakdown voltages (>200V) in GaN-based HFET with high channel sheet charge (>10<sup>13</sup> cm<sup>-2</sup>)?* p. 131  
 I. Daumiller, P. Schmid, E. Strobel, and E. Kohn  
 University of Ulm, Ulm, Germany
- *Biologically weighted UV-meters based on AlGaIn schottky barrier photodetector* p. 133  
 E. Monroy, F. Calle, E. Muñoz, F. Omnès, and P. Gibart  
 ETSI Telecomunicación, Madrid, Spain  
 CRHEA-CNRS, Valbonne, France

## Group III-Nitride Semiconductor Transistors for Power Amplifiers

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**ABSTRACT:** AlGaN-based transistors for microwave power amplifiers have achieved power results exceeding GaAs technology by a factor of five at 10 GHz. These results are due to improved material and device technologies. This paper reviews the rapidly advancing state-of-the-art for these devices and outlines future directions.

### INTRODUCTION:

The group III-Nitride semiconductors, namely InN, GaN, AlN, and their alloys, have been recognized as ideal candidates for high power, high temperature, and/or high frequency electronic devices. This result from their wide bandgap, high breakdown field, high electron velocity, and respectable thermal conductivity. Table I lists three figures-of-merit (FOM) developed to compare the microwave transistor performance based on various material systems. Both the Johnson FOM and Baliga High Frequency FOM show the clear potential of GaN based technology with a 10 to greater than 100 fold increase over GaAs and InP devices.<sup>1,2</sup> The Keyes FOM, which addresses thermal limitations, shows the advantage of SiC technology for thermal management.<sup>3</sup> The GaN technology, however, can be grown on SiC to also give the GaN device the thermal advantage as noted in the footnote of Table I. The advantage of GaN-based transistors over that of SiC stems from its high critical breakdown field (3.3 MV versus 2 MV) and heterostructure capability. The later, allowing the creation of a 2 Dimension Electron Gas (2DEG) affords higher carrier mobility and better carrier confinement that in turn gives higher gain, higher efficiency, and better linearity.

**Table I**

Microwave power transistor figures-of-merit (FOMs) for several candidate semiconductor materials (Johnson's, Keyes', and Baliga's High Frequency FOMs)<sup>1,2,3</sup>

|   | Si | GaAs | InP  | 4H SiC | GaN  |
|---|----|------|------|--------|------|
| JFOM: $(E_c v_{sat}/\pi)^2$               | 1  | 1.7  | 2.8  | 178    | 272  |
| KFOM: $\lambda(v_{sat}/\epsilon_r)^{1/2}$ | 1  | 0.32 | 0.45 | 4.6    | 1.4* |
| BHFFOM: $\mu E_c^2$                       | 1  | 11   | 10   | 27     | 178  |

\* for growth on SiC, the thermal conductivity of SiC is used and this becomes 4.2

Despite these advantageous attributes, until recently, little effort had been directed towards realizing high performance electronic devices in AlGaIn materials. This was solely due to the difficulty in synthesizing high quality bulk or hetero-epitaxial material. This is now rapidly changing.

#### **AlGaIn HEMT STATE-OF-THE-ART:**

From the rudimentary GaN and AlGaIn transistor developments in the early 1990's, high power, high frequency devices are now being reported. While the best hero results are being surpassed on a regular basis, some of the best metrics to date from AlGaIn/GaN high electron mobility transistors (HEMTs) include: a power density of 6.8 W/mm at 10 GHz (3.1 W/mm at 18 GHz); a total power of 9.1 W from a 3 mm device at 7.5 GHz; 53 % PAE and 5.5 W at 4 GHz from a large gate (0.7  $\mu$ m) device; 62 % PAE 3.2 W/mm and 13.9 dB gain at 10 GHz; 78% PAE and 2.7 watts at 4 GHz:  $f_t$  of 75 GHz; and  $f_{max}$  of 140 GHz.<sup>4,5,6,7,8</sup> These results, while below the theoretical limit for this material system, point to the dramatic improvements that are possible over GaAs or InP-based technologies that typically are limited to ~1 W/mm at 10 GHz.

The next step is to continue to push the total power and the efficiency up to compete for satellite and mobile communications applications. This will require improvements in material uniformity and reductions in trapping effect. Traps in AlGaIn/GaN HEMTs that give rise to rf current and gain compression were first reported by Binari, et al., and is now reported in devices from many different laboratories.<sup>9</sup> The nature of the traps is under investigation but they are most likely at the epilayer/substrate interface or in the AlGaIn barrier. Reduction of trap effects is being addressed from fundamental materials studies (e. g. reduction of extrinsic and intrinsic defects) as well as with device design (optimizing the Al-composition and barrier thickness).

Additional work is addressing the circuit advantages of the higher power per unit capacitance (W/pF) and higher operating voltage of these devices. The former enables wide band operation while the later affords more efficient power combining due to the higher impedance level. The first GaN-based amplifier has been reported using a flip-chip hybrid approach with a single 2 mm AlGaIn/GaN HEMT and achieved 35 dBm (3.2 W) of output power over 4-8 GHz with a PAE of 14 to 21%.<sup>10</sup> This output power is a factor of 2-3 higher than that achieved from GaAs-based technology using a similar size device but was still 2-3 times below the design goal of 6-9 W. The shortfall was ascribed to the use of the use of non-optimized transistors.

#### **AlGaIn/GaN HETEROJUNCTION BIPOLAR TRANSISTORS:**

Clearly the group III-Nitride microwave HEMTs are making dramatic advances, however, this material system promises much more. The first AlGaIn/GaN heterojunction bipolar transistors (HBTs), while of modest performance, have now been demonstrated.<sup>11</sup> III-Nitride HBTs promise high linearity, low phase noise, and high power densities. These early HBTs were limited by high base access resistance due to the difficulty in achieving low p-type resistivity. This is a result of the large acceptor ionization energy (>170 meV) in GaN and the limited solubility of the acceptor species (typically Mg) in

the host lattice. This results in a base sheet resistance of  $>10\text{k}\Omega/\text{sq}$  and poor, or even non-ohmic, base contacts. While work on alternative p-doping approaches is ongoing, some of the base resistance problem can be mitigated by aggressive device scaling of the emitter dimension. For example, a 10 times reduction in the emitter width is equivalent to a 100 fold reduction in base access resistance. For this case, with present AlGaIn/GaN material parameters, a 50 V breakdown HBT was predicted to have a  $f_t$  of 50 GHz and a  $f_{\text{max}}$  of 70 GHz.<sup>12</sup> Such a device would dramatically reduce the phase noise in an X-band radar and thereby potentially improve the system sensitivity by over 60 dB.

### **PUSHING TO mm-WAVE OPERATION:**

The majority of the work on group III-Nitride transistors has been focused on operation at 1 to 20 GHz. Significant commercial and military applications exist at least up to 35 GHz, hence there is a market pull to increase the frequency of operation of this technology. One approach to this is to develop a pseudomorphic technology as done in the AlGaAs/InGaAs system by using InGaN channels. This is expected to give better carrier confinement and enhanced electron velocity. The material challenges for the approach are formidable as InGaN tends to phase segregate unless maintained at a low growth temperature. Hence, overgrowth of the barrier layer, either AlGaIn, GaN, or InAlGaIn, can be expected to degrade the quality of the InGaN channel. This may be an opportunity for MBE growth, as opposed to the more widely applied MOCVD growth, to play a role to optimize these structures due to its lower growth temperature.

### **SUMMARY:**

The status of AlGaIn/GaN HEMTs has been reviewed. This technology is rapidly advancing and is expected to see market acceptance around 2005. Future opportunities exist for developing group III-Nitride based HBTs and pushing the HEMT technologies to higher frequencies with In-containing channels. The dramatic improvements in power density and efficiency should enable new solid state communication, guidance, and radar systems.

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23rd Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE '99),  
Chantilly, France, May 26-28, 1999

## MOCVD Grown AlN/GaN HFETs

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GaN-based heterojunction FETs (HFETs) have demonstrated good high frequency and high power performance. AlGaIn/GaN HEMTs grown on SiC were recently reported with a record power density of 5.3W/mm at 10GHz and a high output power of 4W from 2mm discrete devices<sup>1</sup>. The power capability can be further enhanced by means of increasing the Al fraction in the donor layer and a record power density of 3W/mm at 18GHz has been reported using Al<sub>0.5</sub>Ga<sub>0.5</sub>N/GaN HEMTs grown on sapphire<sup>2</sup>. The advantages of Al-rich donor layers stem from the possibility of higher electron mobility and increased surface density of the two-dimensional electron gas (2DEG) at the interface of AlGaIn and GaN<sup>3</sup>. These need, however, to be considered in conjunction with piezoelectric effects that are very pronounced in GaN-based devices. The AlN/GaN approach explored in this work opens the possibility of utilizing devices with a very wide bandgap material under the gate and thus good microwave power performance. Approaches of this type with more traditional III-V semiconductors allowed obtaining large power density and high operation frequency up to the millimeter-wave.

Success of AlN/GaN HFET approaches critically depends on developing material with good structural properties and low density of interface states. AlN and GaN present lattice constants mismatch and thus the thickness of the AlN barrier should be kept below the critical thickness in order to minimize the number of dislocations. Moreover, results reported so far suggest mediocre interface roughness probably related to inter-diffusion between Al and Ga. However, electrical characterization performed on samples used in this work show good interface characteristics. The study of the GaN-based single-heterojunction FETs (HFETs) that are reported in this paper also demonstrates that results using thin AlN barriers to allow improved current capability and charge control are very promising.

The AlN/GaN layers were grown by low-pressure (60torr) MOVPE at the University of Michigan using TMGa, TMAI, and NH<sub>3</sub> as precursors. The device cross-section is shown in Fig. 1. Starting from the c-plane sapphire substrate one distinguishes a thin low-temperature (515°C) grown GaN buffer layer, a 0.5μm-thick non-intentionally-doped GaN channel, and a thin AlN barrier layer. All layers were grown at 1120°C. The AlN/GaN layer design was optimized by evaluating the mobility dependence on AlN layer thickness as obtained by Hall measurements as shown in Fig. 2. When the thickness of the AlN layer was ~110Å, the combined bulk-2DEG electron mobility was 320cm<sup>2</sup>/Vs and associated 2DEG density was 2×10<sup>13</sup>cm<sup>-2</sup>, respectively. This design was used in the device study as it represents the best conditions for good interface properties and best carrier-density conditions in the channel.

AlN/GaN HFETs were fabricated on these structures using Cl-based dry etching for device isolation and Ti/Al/Ti/Pt and Pt/Ti/Au metals for ohmic and gate contacts, respectively. The ohmic metals have been annealed for 30sec at 800°C in nitrogen. Devices with a gate length of 2μm exhibited a peak transconductance of 136mS/mm at V<sub>GS</sub>=1V, which exceeds previously reported results. The threshold voltage of the devices was -3.5V and the maximum drain current was greater than 700mA/mm. Drain-source breakdown at 30V and drain-gate breakdown at 40V were evidenced by flashing of the contact pads. Gate leakage current present at large gate and drain bias was due to parasitic conductance in the N.I.D.-GaN layer. Overall, we investigated AlN/GaN heterostructures using thin epitaxially grown AlN barrier layers and obtained very high values of transconductance and current density from HFETs fabricated on such materials. These results indicate a high potential of AlN/GaN HFETs for microwave power applications.

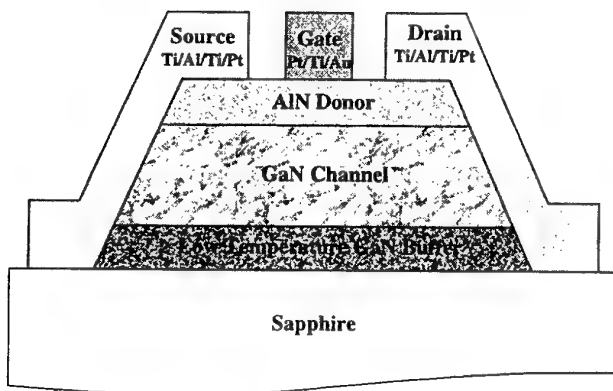


Figure 1: Cross-sectional view of AlN/GaN HFET shows low-temperature grown GaN buffer, 0.5μm-thick GaN channel, and 10nm-thick AlN barrier layers. The device mesas were etched by Cl-based RIE. Ohmic and gate contacts were made with Ti/Al/Ti/Pt and Pt/Ti/Au, respectively.

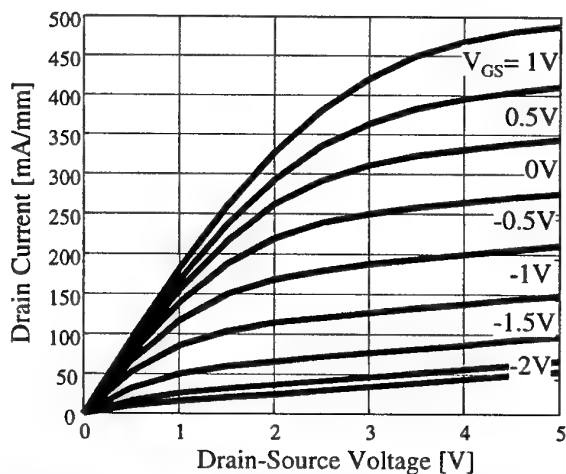


Figure 3:  $I_D$ - $V_{DS}$  characteristics of AlN/GaN HFETs with 2μm-long gate. Maximum current density for device shown is 560mA/mm at  $V_{DS}=15V$ .

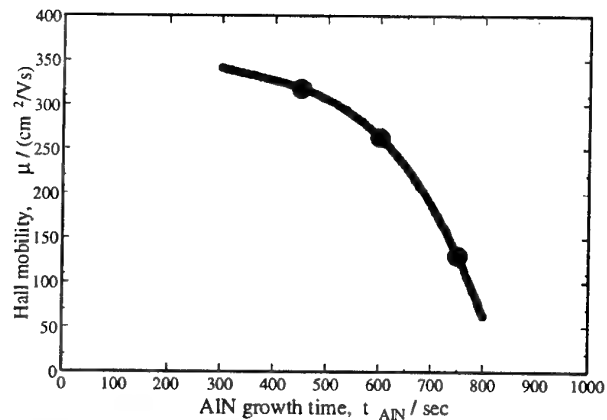


Figure 2: Dependence of electron mobility on the thickness of the AlN barrier layer.

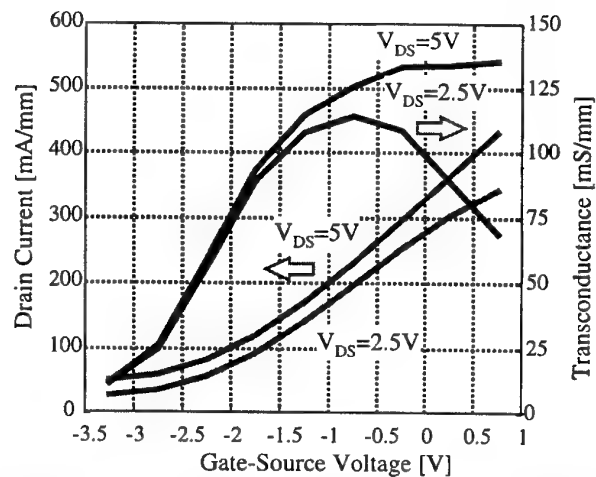


Figure 4: Transfer Characteristics of AlN/GaN HFET shown in Fig. 2. Peak transconductance of 136mS/mm occurred at  $V_{GS}=1.0V$  and  $V_{DS}=5V$ .

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# Single and double barrier AlGaIn/GaN modulation doped field effect transistors grown by RF assisted MBE

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We have analysed the DC and small signal RF performance of single and double barrier heterostructure AlGaIn/GaN MODFETs. The fabricated structures were grown by RF assisted MBE on sapphire and include an AlN nucleation layer, a 1  $\mu\text{m}$  thick unintentionally doped (UID) GaN buffer layer, followed by a 3nm UID-AlGaIn spacer layer, 10nm Si doped (nominally  $1 \times 10^{19} \text{cm}^{-3}$ ) AlGaIn supply layer and finally a 10nm UID-AlGaIn cap layer. The double barrier FET (DB-MODFET) includes an additional 35nm UID AlGaIn layer placed in such way, that a 35nm GaN channel is formed. The Al content in all AlGaIn layers was 15%. Hall measurements were performed at various positions across the 2" wafers yielding a good homogeneity of the electrical properties, which is also reflected in the uniform device performance across the wafers. The conventional MODFET structure yields a best mobility value of  $520 \text{cm}^2/\text{Vs}$  at a sheet concentration of  $7.5 \times 10^{12} \text{cm}^{-2}$ . For the DB-MODFET structure values of  $\mu = 450 \text{cm}^2/\text{Vs}$  and  $n_s = 6.5 \times 10^{12} \text{cm}^{-2}$  were extracted.

Devices were fabricated on these layers using standard RIE for mesa etching and Ti/Al/Ni/Au for the ohmic contacts, which were annealed in  $\text{N}_2$  at  $900^\circ\text{C}$  for 30s. The contact resistance was  $1 \Omega\text{mm}$  for the conventional structure and approx.  $2 \Omega\text{mm}$  on the DB-MODFET sample. Electron beam lithography was used to define  $0.3 \mu\text{m}$  T-shaped gate contacts (Pt/Au).

The output and transfer characteristics characteristics of devices with a gate width of  $100 \mu\text{m}$  are shown in Figs. 2 and 3. For both structures a maximum drain current of approx.  $550 \text{mA/mm}$  is reached. However, due to the higher sheet and contact resistance the DB-MODFET structure yield a higher knee voltage of almost 9V. The higher series resistance results also in reduced maximum transconductance of approx.  $125 \text{mS/mm}$ , as compared to the conventional MODFET with  $g_{m\text{ext}} = 150 \text{mS/mm}$ . The intrinsic transconductance, calculated according to  $g_{mi} = g_{m\text{ext}} / (1 - R_s * g_{m\text{ext}})$ , yield for both structures approx.  $190 \text{mS/mm}$ .

For gate voltages lower than -3V the output characteristics of the DB-MODFET shows a nonlinear behaviour (at small  $V_{ds}$ ) and a reduced modulation efficiency of the output current with gate bias. This effect is reflected in the transfer characteristics by a reduced slope. Also a second maximum of the transconductance at approx.  $V_{gs} \approx -4.8 \text{V}$  is observed. This effect could be explained by a parallel conducting path, which is located at the second AlGaIn/GaN interface. This is supported by the observation that the ratio of the two transconductance maxima ( $g_{m-4.8\text{V}}/g_{m-0.9\text{V}} \approx 0.28$ ) is similar to the depth ratio of the two channels ( $23 \text{nm}/93 \text{nm} \approx 0.25$ ).

The RF-performance of the fabricated devices is shown in Fig. 4. The conventional MODFET structure yields  $f_t \approx 30 \text{GHz}$  and  $f_{max} \approx 45 \text{GHz}$ . The DB-MODFET shows reduced  $f_t$  and  $f_{max}$  probably due to the poorly modulated second conducting channel.

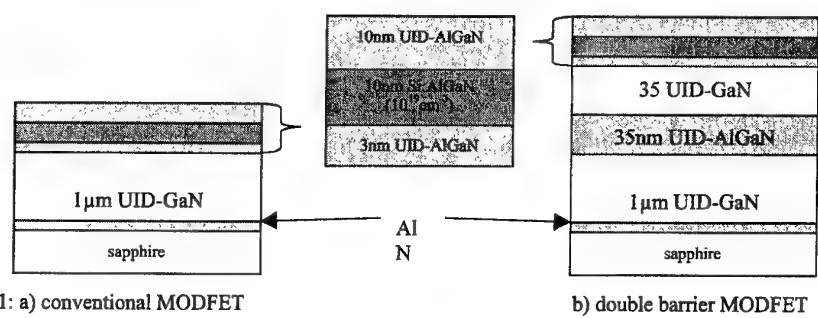


Fig. 1: a) conventional MODFET

b) double barrier MODFET

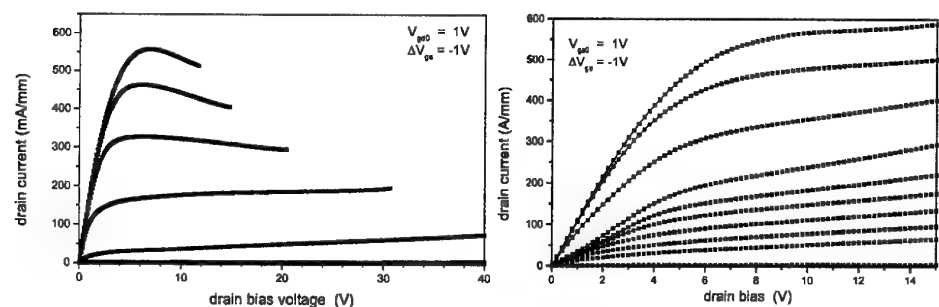


Fig 2: Output characteristics of: a) conventional MODFET

b) double barrier MODFET

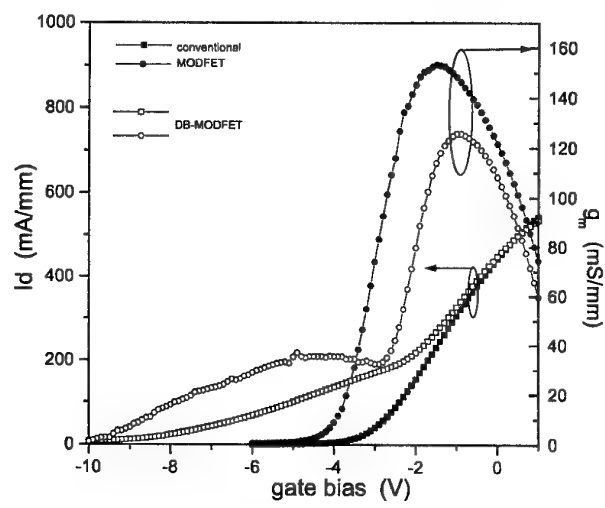


Fig 3: Transfer characteristics and transconductance

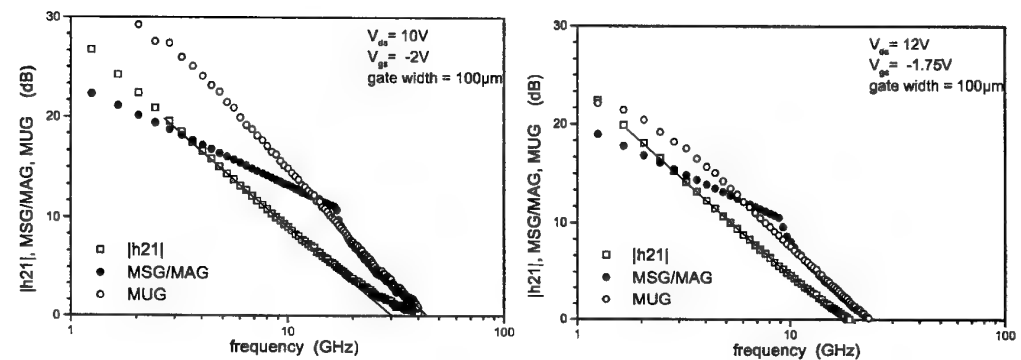


Fig 4: RF performance of : a) conventional MODFET

b) double barrier MODFET

## GaN Static Induction Transistor Fabrication

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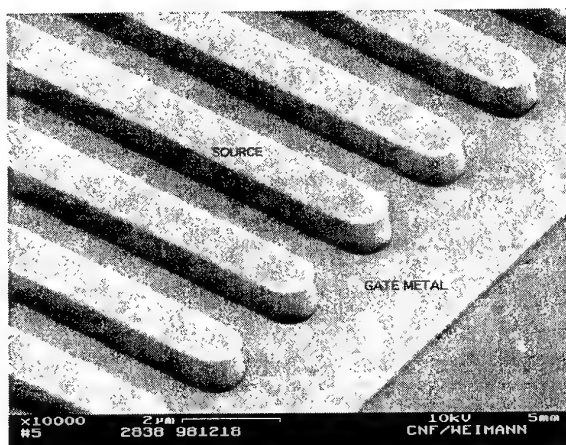
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The GaN Static Induction Transistor (SIT) is a promising high-power, high-frequency semiconductor device. Its SiC counterpart has a proven high power capability; modules delivering 1 kW at 800 MHz are commercially available by now. AlGaIn/GaN High Electron Mobility Transistors (HEMT's) have shown excellent frequency performance. Using GaN as a semiconductor material for SIT's, we try to combine the high power handling capability of a SIT device structure with the good transport properties of GaN. We report on the GaN Static Induction Transistor process development, latest device results will be presented.

Contrary to the AlGaIn/GaN HEMT, the GaN SIT requires development of etch processes for the gate recess, and to access the buried drain layer. The design of the Static Induction Transistor required two-dimensional drift-diffusion simulation of the coupled Poisson- and carrier continuity equations, to optimize the device geometry for a given carrier concentration in the epilayer. The GaN SIT is scaleable with regards to frequency performance and power; a thicker drift region can be used for higher operating voltages, while a higher doping concentration will lead to a higher cutoff frequency. Our design is optimized for high-power operation at X-band.



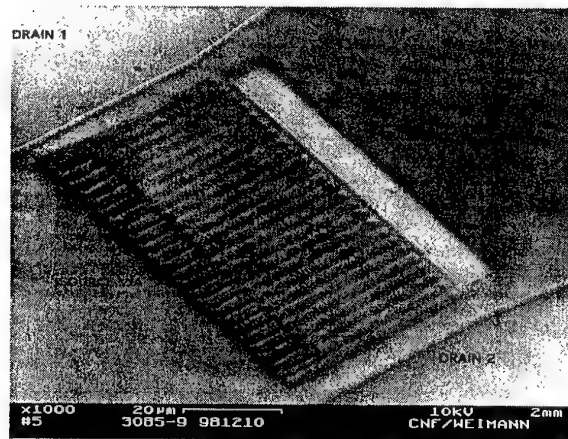
**Figure 1: self-aligned multi-finger GaN SIT structure after gate metal deposition**

We successfully transferred optical stepper lithography processes to the application with transparent substrates such as Sapphire and SiC, with minimum linewidths of  $.7 \mu\text{m}$  (lift-

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off process). Recent work focused on the realization of an etch process for self-aligned gate fabrication, with the achievement of gate-source isolation. A combined ECR dry etch and hot KOH wet etch was the key to reproducible fabrication of perfectly vertical GaN structures. Etch depths of 1  $\mu\text{m}$  and feature widths down to 0.7  $\mu\text{m}$  were realized, with excellent sidewall roughness. This etch process could be adapted to the fabrication of laser bars, as well. The perfect verticality of the sidewalls enabled us to evaporate self-aligned Schottky gates. Test diodes were successfully fabricated, using Ni as a Schottky metal on the etched GaN surfaces. Breakdown occurred at 25V applied between gate and drain.

Although the SIT is a vertical device, with a buried drain contact accessible via a conducting substrate ( $n^+$  SiC) from the back of the substrate, the constrained availability of thick GaN layers on SiC led us to the development of top-accessed ohmic drain contacts. A second ECR etch process, yielding a sidewall slope of  $45^\circ$ , was developed to etch 2  $\mu\text{m}$  deep, down to the drain contact layer, using 5  $\mu\text{m}$  thick photoresist as an etch mask. Both drain and source ohmic contacts are based on a Hf/Au metallization. Without annealing, this contact metallization yields a reasonable contact resistance  $<10\text{-}5\ \Omega\text{cm}^2$ , as measured by circular TLM.



**Figure 2: passivated device structure**

A bridging process is needed to connect the tops of the source fingers to the source contact pad. In a first attempt, we used PECVD  $\text{SiN}_x$  to planarize the device structure prior to dry etching of via holes on top of the source fingers and subsequent deposition of the interconnect metal. Large pinhole concentration and enhanced etching of the  $\text{SiN}_x$  along the sidewalls of the exposed source pillars led to shorts between the gate and the source. Currently we use a two-step polyimide planarization process, with a self-aligned RIE etch step to expose the source fingers.

# GaN MESFETs for high temperature applications

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The GaN-based materials system has outstanding electronic properties. Its wide bandgap (3.4 eV at room temperature) is a great advantage for power and high temperature applications.

First of all, we will show the stability of the Ti/Al/Ni/Au ohmic contact and Pt/Au Schottky contact with the temperature. Then, measurements of a MESFET will be presented under high temperature static conditions. Finally, temperature pulsed measurements performed under DC and RF conditions will be analysed.

To study the ohmic contact stability, Ti/Al/Ni/Au (150/2200/400/500 Å) metallization layers are evaporated on a 2 µm thick GaN layer grown by Metal Organic Chemical Vapour Deposition (MOCVD) on a sapphire substrate and doped with Si at  $5 \cdot 10^{17} \text{ cm}^{-3}$ . This contact is annealed under nitrogen atmosphere at 900 °C during 30 s. Then, the samples are put in an oven at different temperatures. We observe that this ohmic contact is stable until 600 °C (see figure 1). We will show a similar study concerning Schottky contact.

The MESFETs have been processed on epilayers grown by MOCVD on a (0001) sapphire substrate. It consists of a 250 Å GaN nucleation layer, a 3.6 µm GaN undoped layer and a 2000 Å Si-doped GaN active layer. Hall measurements give a doping level of about  $2.7 \cdot 10^{17} \text{ cm}^{-3}$  and a hall mobility of 330 cm<sup>2</sup>/Vs at room temperature. Then, the ohmic contacts studied above are deposited and the mesa is performed by Reactive Ion Etching with SiCl<sub>4</sub> gas. The gate length of 0.3 µm is defined by electron beam lithography. It is made of Pt/Au (100/1000 Å). The device has a 2×50 µm wide gate and the source to drain spacing is 2.3 µm. It exhibits 260 mA/mm under static conditions at a drain to source voltage V<sub>ds</sub> of 18 V and a gate to source voltage V<sub>gs</sub> of 1 V.

The figure 2 exhibits the pulsed I-V characteristics performed on the same device at room temperature (plain line) and at 150 °C (dotted line) for V<sub>ds0</sub>=18 V and V<sub>gs0</sub>=-9 V. The maximum drain current observed at room temperature is 120 mA/mm at V<sub>ds</sub>=18 V and V<sub>gs</sub>=1 V, which is less

than a half of the current obtained under static conditions. This loss can be explained by the existence of electrical traps localised in the material or/and at the surface. Indeed, at 150 °C, the maximum drain current is 220 mA/mm at  $V_{ds}=18$  V and  $V_{gs}=1$  V. This value is nearly the same as under static conditions because electrons can be untrapped owing to the temperature and then participate to the conduction.

These electrical traps degrade the performances of the device at low temperature. On the opposite, at high temperature, the electrical performances are improved. This is suitable for high temperature applications.

Acknowledgement : the layers were provided by Thomson CSF-LCR. This work has been carried out with the financial help of the DGA (French Army), Contract No. 97-065, the Conseil Régional du Nord and the CNRS.

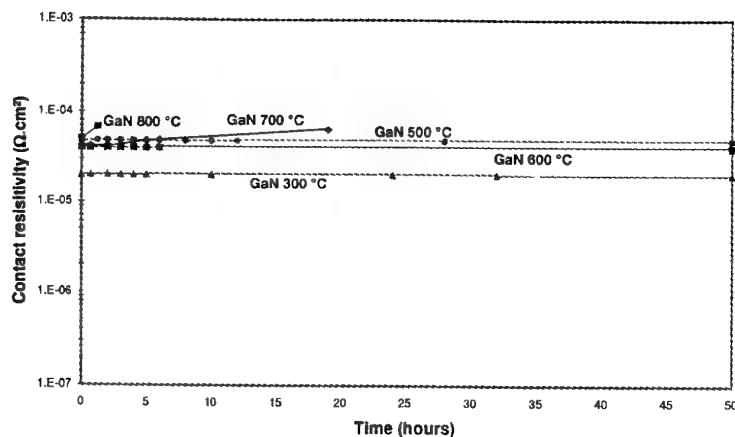


Figure 1 : stability of the Ti/Al/Ni/Au ohmic contact over the time for different temperatures.

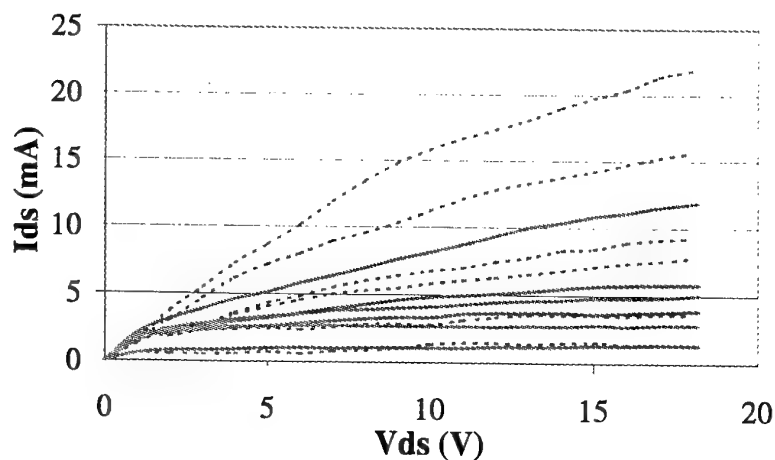


Figure 2 : pulsed I-V characteristics at 20 °C (plain line) and 150 °C (dotted line) for  $V_{gs}$  from 1 V to -9 V (step -2 V).

23rd Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE '99)  
Chantilly, France, May 26-28, 1999

## Power Performance of AlGaIn/GaN HEMTs with 0.2 to 1mm Gate Widths

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The high-power characteristics of GaN/AlGaIn HEMTs have attracted a lot of interest because of the emerging needs for high-power microwave amplifiers in various applications such as wireless base stations, satellite communication, and defense electronics. The demonstration of AlGaIn/GaN HEMTs with high drain-source breakdown of 100V and  $f_{MAX}$  of 80GHz [1] indicated the excellent potential of these devices for microwave power applications. Moreover, the aptitude of GaN-based HEMTs for microwave power applications has been confirmed by recent reports of record power density of 3W/mm at 18GHz [2] and 5.3W/mm at 10GHz [3]. However, detailed investigations of the power performance and large-signal properties of large-periphery devices are still necessary to fully explore the potential of AlGaIn/GaN HEMTs. In this work, high-frequency power characteristics of large-periphery AlGaIn/GaN HEMTs are obtained using an automatic load-pull system and discussed together with DC and small-signal high-frequency characteristics.

AlGaIn/GaN HEMTs with 0.25 $\mu$ m-long gates were fabricated on layers grown by RF-assisted MBE on sapphire substrates. A cross-sectional view of the layer structure is shown in Fig.1. The growth and fabrication details have been reported elsewhere [1]. Thick Au-plated contact pads were used in these devices to reduce self-heating. HEMTs with gate widths ranging from 200 $\mu$ m to 1mm have been investigated. Typical  $I_D$ - $V_{DS}$  characteristics presented  $I_{DSS} \approx 500$ mA/mm and  $g_m \approx 100$ mS/mm (Fig.2). The cutoff frequency  $f_T$  and maximum oscillation frequency  $f_{MAX}$  were 27GHz and 45GHz, respectively. Maximum  $f_T$  and  $f_{MAX}$  occurred for  $V_{GS}$  of -5V and  $V_{DS}$  of 15 V.

The large-signal properties of AlGaIn/GaN HEMTs were studied at 8GHz using a computer-controlled on-wafer load-pull system with electromechanical tuners. Both input and output tuners were positioned to obtain the best gain. Devices with 1-mm gate width demonstrated maximum output power (30dBm), PAE (28%), and gain (17.6dB) when the gate and drain bias were set to -6.75V and 15V respectively. In addition, a higher power density of 1.3W/mm and a slightly improved PAE of 32% were obtained using 600 $\mu$ m-wide HEMTs.

AlGaIn/GaN HEMTs with different gate width demonstrated excellent scalability of power properties. In particular, it was observed that as the gate width varied from 200 $\mu$ m to 1.0mm, the input power at 1dB gain compression increased proportionally demonstrating therefore delayed onset of gain compression. At the same time the output power also increased while the output power density, power-added-efficiency and gain remained in general constant.

Overall, high output power and power-added efficiency were obtained from 1mm-wide AlGaIn/GaN HEMTs indicating the high potential of GaN-based technology for power microwave amplification and good large-signal scaling properties are reported.

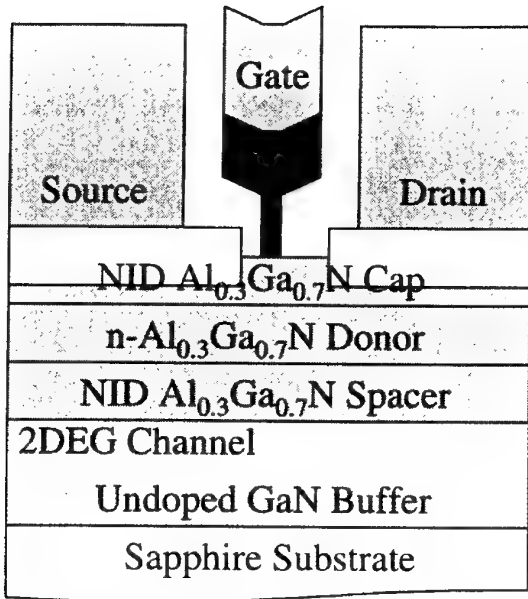


Fig.1. Cross-section of AlGaIn/GaN HEMT indicating 2 $\mu$ m-thick NID GaN buffer, 3nm-thick NID Al<sub>0.3</sub>Ga<sub>0.7</sub>N spacer, 20nm-thick Al<sub>0.3</sub>Ga<sub>0.7</sub>N donor doped at  $2 \times 10^{18} \text{ cm}^{-3}$ , and 15nm-thick NID Al<sub>0.3</sub>Ga<sub>0.7</sub>N cap, and the contacts

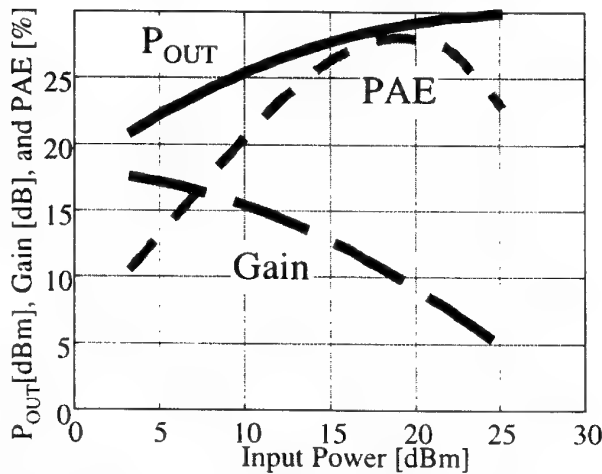


Fig.3. Power saturation characteristics of AlGaIn/GaN HEMTs with 1mm wide gate. Source and output tuners were optimized for maximum gain of 17dB at 8GHz. Maximum output power was 1W. HEMTs demonstrated the output power density of 1W/mm and maximum PAE of 28% with associated gain of 10dB at the input power of 17dBm.

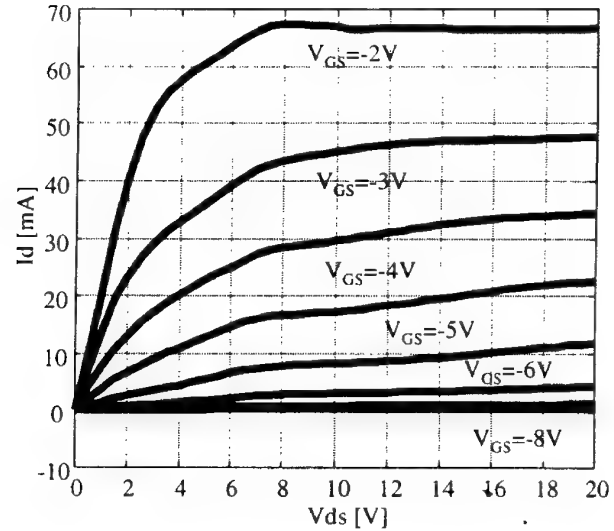


Fig.2.  $I_{DS}$ - $V_{DS}$  characteristics are shown for AlGaIn/GaN HEMT with 200 $\mu$ m wide gate. HEMT had  $I_{DSS}=0.5\text{A/mm}$  and maximum  $g_M=100\text{mS/mm}$ . Pinch-off voltage was -8V

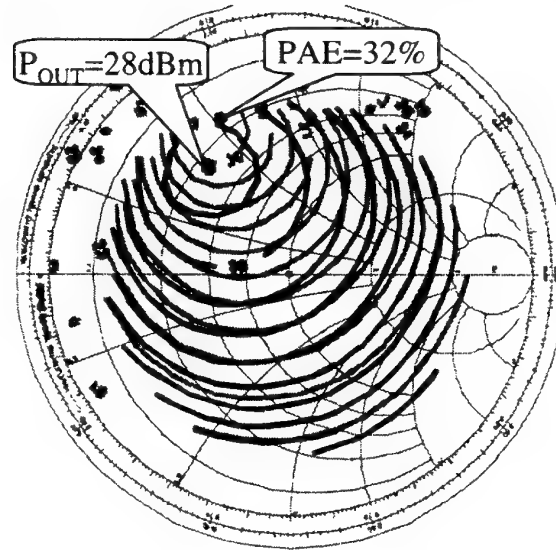


Fig.4. Constant output power and constant power-added efficiency contours were evaluated for 8-finger AlGaIn/GaN HEMTs under high input power conditions (22dBm). The position of optimal loads for maximum  $P_{OUT}$  (28dBm) and maximum PAE (33%) are located close to each other on the Smith Chart.

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## How to Explain the High Breakdown Voltages ( $\geq 200\text{V}$ ) in GaN-Based HFET With High Channel Sheet Charge ( $\geq 10^{13}\text{cm}^{-2}$ )?

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In contrast to classical semiconductor FET devices the characteristics of GaN-based FETs show in many cases unexpected high breakdown voltages in combination with high sheet charge densities. Gate-drain breakdown voltage of more than 400 V and three terminal breakdown voltages above 200 V have been reported, the later in combination with an open channel sheet charge of  $1.2 \cdot 10^{13}\text{cm}^{-2}$ [1][2]. Also, in these devices the dependence of the gate-drain breakdown voltage with gate-drain spacing is a common phenomenon, a linear relationship being reported in [2]. Another characteristic of many GaN-based FET devices is the discrepancy between RF power density and quasistatic power density, the RF power being only a fraction of the quasi-static power. Up to now there is no model available to explain all three phenomena consistently. In this contribution such a model will be proposed. It is illustrated with fig.1.

In classical heterostructure FET devices with 2DEG channel the extension of the gate-drain high field region is governed by the Schottky layer depletion characteristics. Thus, the lateral field is largely linearly decreasing from the gate edge onwards. In the case a gate to drain separation of  $\mu\text{m}$ -scale the drift region will not reach the drain contact even at breakdown and the breakdown voltage is not dependent on the spacing. In this case the product of channel sheet charge density and maximum drain voltage is a constant and the penalty for a high breakdown voltage is a low open channel current density [3].

The observation that the gate to drain breakdown voltage is linearly related to the gate-drain spacing may imply a constant field between both contacts. Then, this is typical for breakdown between the two contacts of a capacitor or a resistor structure with neglectable net charge in the contact separation layer. Such a medium may be considered a lossy dielectric acting capacitively at high frequency and resistive at low frequency, the transition occurring at the dielectric relaxation cutoff frequency  $1/\tau = \sigma/\epsilon$ .

To explain the above mentioned phenomena in the FET structure, it may thus be assumed that a lossy dielectric layer is acting in parallel to the channel (and the 2DEG supply layer in case of a MODFET structure), however separated by a barrier to allow gate control. In such an arrangement a vertical voltage drop will develop between the two layers causing a vertical dipole to build up, if the FET is operated in saturation and a drift region is developed as indicated in fig.1. As a consequence, the channel donor charge (or channel supply donor charge) is vertically compensated and the gate to drain region effectively neutralized.

Then the gate to drain breakdown voltage becomes dependent on the gate to drain spacing and an average breakdown field may be extracted. However, the lossy dielectric layer should not short-circuit the gate to drain drift region and should not degrade the output conductance. Thus, it needs to be of high resistance. As a consequence, the dielectric relaxation cutoff frequency will be low and the negative charge in this layer (compensating the channel donor charge) can only be removed with the corresponding delay. The charge not removed fast enough will represent a negatively charged second gate and act as a current limiter, reducing the maximum RF output power. Thus, a quasi-static gate to drain breakdown voltage, which depends on the (micrometer-scale) gate to drain spacing cannot be used to assess the RF maximum power density in these devices. Moreover, the devices will be plagued with a frequency dispersion.

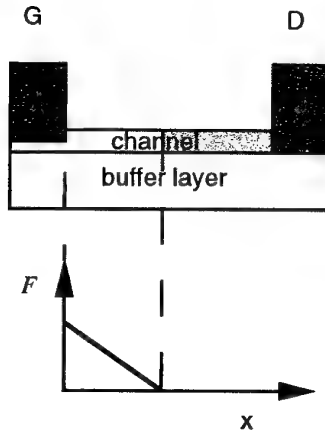
The model can explain the electrical phenomena correctly, does however not allow to draw a conclusion on the physical/chemical origin of the lossy dielectric layer.

### LITERATUR

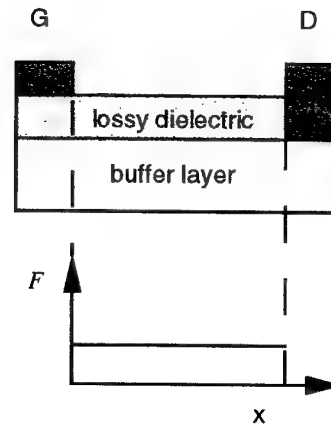
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Fig.1: Illustration of new concept

## Conventional FET structure



## Lossy dielectric (LD) channel



drift region (+) charged

linear field distribution across drift region

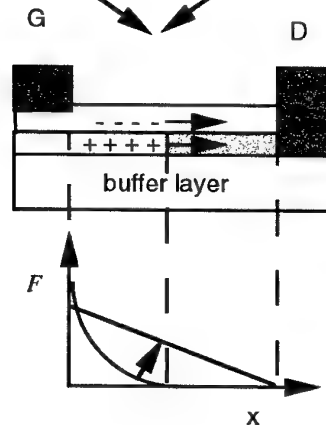
$V_{GDmax}$  not dependent on GD-separation (for  $\mu m$ -size  $L_{GD}$ )

GD-separation represents neutral region

constant field across GD-separation

$V_{GDmax(LD)}$  linearly dependent on GD-separation

in LD-HFET:



$V_{GDmax(LD)}$  dependent on GD-separation

modulation of charge in GD-region only with  $\tau = \epsilon/\sigma$

$V_{GDmax(LD)}$  not relevant for RF power density

## Biologically Weighted UV-meters Based on AlGa<sub>x</sub>N Schottky Barrier Photodetectors

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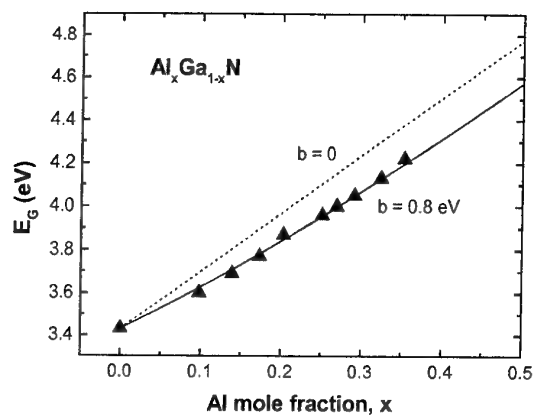
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In the last years, the monitorization of the solar UV radiation has become a priority topic for the scientific community, due to the depletion of the stratospheric ozone layer. The important effects of the solar UV-B (320-280 nm) and UV-A (400-320 nm) bands on the ecosystem and on human health justify the research to develop accurate, compact, low-cost UV meters. Radiometric UV measurements have been traditionally accomplished by photomultiplier tubes, but these instruments are expensive, physically fragile, and require high power supplies. In order to evaluate the possible damage induced by the solar UV band on the human health, more compact and user-friendly meters have been developed, consisting of narrow-bandgap semiconductor photodiodes. These systems offer the advantages of small, solid-state devices, requiring only a moderate bias voltage. However, the well-established materials (Si, GaAs, GaAsP) have bandgaps far below 3.1 eV (400 nm), so that external filtering is needed to block out the visible and infrared radiations. Moreover, narrow-bandgap semiconductors are quite sensitive to temperature variations, so that a Peltier system is required to stabilize the temperature of the device. By proper design of filters and phosphor coatings, the detector response can simulate the erythema action [1].

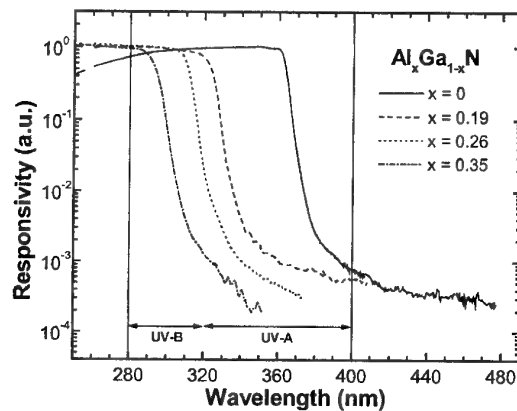
In this work we demonstrate that the Al<sub>x</sub>Ga<sub>1-x</sub>N family of wide-bandgap semiconductors makes possible the fabrication of photodetectors whose output current is proportional to the UV irradiance weighted by the erythema action spectrum. Al<sub>x</sub>Ga<sub>1-x</sub>N alloys are the ideal choice for visible-blind UV detection [2]. They present the advantage of a direct wide bandgap, which can be tailored from 3.4 eV (365 nm) to 6.2 eV (200 nm) by changing the Al mole fraction. These materials are also remarkably tolerant to aggressive environments, due to its thermal and chemical stability and radiation hardness. The main obstacle to develop nitride UV photodetectors is the difficulty to obtain high quality material, due to the lack of an appropriate substrate for homoepitaxial growth. State-of-the-art GaN still has a high n-type residual doping ( $\sim 10^{16}$  cm<sup>-3</sup>) and a high density of dislocations ( $10^8 - 10^9$  cm<sup>-2</sup>).

Growth of Al<sub>x</sub>Ga<sub>1-x</sub>N ( $0 \leq x \leq 0.35$ ) epitaxial layers on c-oriented by low-pressure metalorganic vapor phase epitaxy has been optimized [3]. Good structural, electrical and optical properties were obtained for both undoped and Si-doped layers. A typical FWHM of 700 arc-sec is measured for the (0002) X-ray double diffraction peak in the  $\omega$ -configuration of AlGa<sub>x</sub>N epilayers, and mobilities of 90 cm<sup>2</sup>/Vs have been obtained in samples with a carrier concentration  $n \approx 10^{18}$  cm<sup>-3</sup>. Optical transmission as well as absorption coefficient measurements using the photothermal deflection spectroscopy have been used to measure the variation of the AlGa<sub>x</sub>N bandgap with the aluminum concentration at room temperature. A bowing parameter of 0.8 eV was obtained (See Fig.1). Planar Schottky photodiodes fabricated on these layers present a linear and fast response, and a UV/visible contrast of  $10^3$  (see Fig. 2) [4]. By proper selection of the Al mole fraction, the erythema action response can be simulated (see Fig. 3).

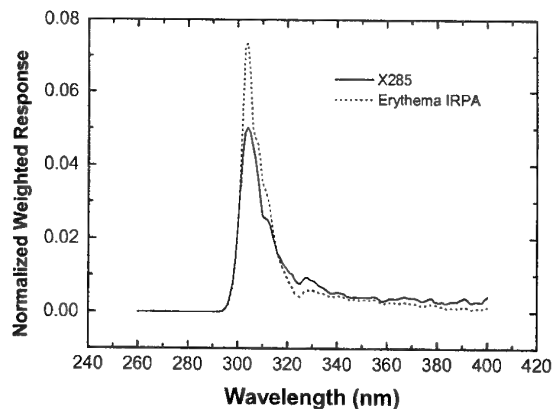
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**Figure 2.** Variation of the  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  bandgap with the Al mole fraction, at room temperature.



**Figure 2.** Spectral response of  $\text{AlGaIn}$  Schottky photodiodes with different Al contents.



**Figure 3.** Spectral response of  $\text{AlGaIn}$  Schottky photodiodes (solid line) and erythema action [5] (dotted line) weighted by the solar spectrum.

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**Friday, May 27, 1999 11:25 am**

## New devices

- *Highly non linear devices for operation at Terahertz frequencies (invited paper)* p. 137  
 Didier Lippens  
 University of Lille-IEMN, Villeneuve d'Acsq, France
- *Resonant Tunneling Diodes for High-Speed Trigger Applications* p. 141  
 F. Yousif, M. Kunze, K. Bitzer, and H. Schumacher  
 University of Ulm, Ulm, Germany
- *A 150 GHz MMIC Receiver Array with On-Chip Pumping-Power Distribution for Plasma ECE Disgnostics* p. 143  
 M. Rodríguez-Gironés, J.P. Pascual<sup>(1)</sup>, M.L. de la Fuente<sup>(1)</sup>, F. Lopez, C.I. Lin, A. Simon, and H.L. Hartnagel  
 Technical University of Darmstadt, Darmstadt, Germany  
<sup>(1)</sup> University of Cantabria, Santander, Spain
- *Hot Electron Injection Field Effect Transistor* p. 145  
 E. Kolmhofer, M. Bergmair, C. Diskus, K. Luebke, A. Stelzer, and H. Thim  
 University of Linz, Linz, Austria
- *Modulation Response Predictions for a Dual Channel SiGe FET* p. 147  
 G.C. Crow and R.A. Abram  
 University of Durham, Durham, United Kingdom
- *Piezoelectric and Optical Properties of Strained InGaAs/GaAs Quantum Well Structures Grown by MOVPE on (111)A GaAs Substrates* p. 149  
 S. Cho, J. Kim, A. Sanz-Hervás, A. Majerfeld, P. Tronc<sup>(1)</sup>, C. Villar<sup>(2)</sup>, B.W. Kim<sup>(3)</sup>  
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Wocsdice'99 May 26-28, Chantilly, France

## Highly Nonlinear devices for operation at Terahertz frequency

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### ABSTRACT

This paper gives an overview of the Terahertz components, currently fabricated at IEMN, which are aimed at operating in THz receivers. This concerns sources, mixers and harmonic multipliers, engineered for ultra-fast electron dynamics and strongly reactive and resistive non linearities. Special attention has been paid to high performance InP-based Heterostructure Barrier Varactors (HBV's) for harmonic multiplication, Double Barrier Heterostructure Resonant Tunnelling Diodes (DBH-RTD's) for fundamental generation and T-gate Schottky's for sub-harmonic mixing. Novel ideas will be presented in order to control the particle and displacement currents and to overcome the intrinsic and extrinsic limitations.

Keywords: Terahertz, Non linear devices, Heterostructure Barrier Varactors, Schottky diodes, Resonant Tunnelling Diodes, oscillators, harmonic multipliers, sub-harmonic mixers

### 1. INTRODUCTION

High speed non linear semiconductor devices are key components for advanced electronic systems in the Terahertz region that handle analogue signals at frequencies typically between 100 GHz and 1 THz. These devices appears vital to the continued growth of this maturing research area which has now a long and respectable history. Recently, tremendous strides have been made which are based on advanced epitaxial and processing techniques including epitaxial and planar integration, the development of heterostructures and the emergence of micromachining techniques. The purpose of this paper is to illustrate this evolution which affects no only the active devices but also their environment and hence the external circuits. The structuring of semiconductors on the micron scale with a high perfection is manifested in a number of important ways. Firstly, one can take advantage of the so called quantum-size effects when the De Broglie wavelength for electron compares to the system dimension. Also, the growth of multi-layered structures opens the way to combine individual samples so that the electrical characteristics can be tailored with respect to the power handling or frequency capabilities notably. To complete our picture of the context, it is also important to mention that advanced processing techniques, including microstructuring of semiconductor dielectric and metallic heterostructures, has brought a profound change in Terahertz technology driven largely by the concern of low cost system development. The devices include Resonant Tunnelling Diodes (RTD's)<sup>1-2</sup> which can operate at room temperature as fundamental solid state source, Heterostructure Barrier Varactors (HBV's)<sup>3-8</sup> which now compete with conventional Schottky varactors for harmonic multiplication, and Heterostructure Schottky diodes<sup>9-11</sup> for Subharmonically pumped mixing.

### 2. RESONANT TUNNELLING DIODES

Resonant Tunneling Diodes are representative of quantum devices operating at room temperature. The generic structure consists of a Double Barrier Heterostructure. This creates a quantum well whose quantum levels can be occupied through a tunneling process. The conjunction of a tunneling process, enhanced by a resonance effect, and of quantum size effects give rise to strong nonlinearity in the current-voltage characteristics with negative differential resistance effects. However, to be observed at room temperature with a significant contrast between the on -resonance and off -resonance states, one of the first requirement is to shrink the barrier dimension in order to increase by this means the quantum probabilities. Also, as a consequence, the life time of trapped carriers on the quasi-bound state becomes very short, on picosecond or subpicosecond scales. This means that the relevant time constant involved in the resonant tunneling process can be kept short with the associated benefit of an intrinsic high frequency capability.

With these requirement in mind, let us now consider pseudomorphic layers which incorporates locally a certain content of Indium increasing by this way the discontinuity between the narrowest gap material and the widest gap compound. Such a band gap engineering via the pseudomorphic growth of InGaAs layer is illustrated in Figure 1 which shows the epitaxial sequence of a resonant tunneling aimed at operating at millimetre wave frequency. The quantum well also contains an InGaAs perturbation and the overall structure can be compared to a triple well double barrier structure.

|                |  |                             |        |
|----------------|--|-----------------------------|--------|
| Contact layer  | In <sub>0.53</sub> Ga <sub>0.47</sub> As | >1x10 <sup>19</sup> at.cm-3 | 5000 Å |
| Cladding layer | In <sub>0.53</sub> Ga <sub>0.47</sub> As | 1x10 <sup>18</sup> at.cm-3  | 1000 Å |
| Spacer         | In <sub>0.53</sub> Ga <sub>0.47</sub> As | n.i.d                       | 50 Å   |
| Barrier        | AlAs                                     | n.i.d                       | 17 Å   |
| Well           | In <sub>0.53</sub> Ga <sub>0.47</sub> As | n.i.d                       | 10 Å   |
|                | InAs                                     | n.i.d                       | 25 Å   |
|                | In <sub>0.53</sub> Ga <sub>0.47</sub> As | n.i.d                       | 10 Å   |
| Barrier        | AlAs                                     | n.i.d                       | 17 Å   |
| Spacer         | In <sub>0.53</sub> Ga <sub>0.47</sub> As | n.i.d                       | 50 Å   |
| Cladding layer | In <sub>0.53</sub> Ga <sub>0.47</sub> As | 1x10 <sup>18</sup> at.cm-3  | 1000 Å |
| Contact layer  | In <sub>0.53</sub> Ga <sub>0.47</sub> As | >1x10 <sup>19</sup> at.cm-3 | 5000 Å |
| Buried layer   | InP                                      | 5x10 <sup>19</sup> at.cm-3  | 5000 Å |

Fe-doped Semi-Insulating InP substrate

Figure 1 Epitaxial sequence for a RTD in InP-based technology

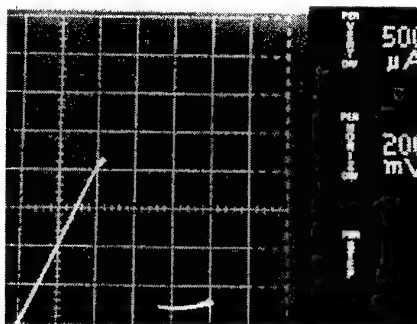


Figure 2: I-V characteristic measured at room temperature for a 1μm² area InP based RTD

The next step in the optimization is the fabrication of the devices which has to be planar integrated. It was early recognized that the conventional whisker-contacted technology cannot be used for a broader application range. Basically, the planar integration of such devices faces two major difficulties. The first one is that the devices has to be integrated by defining small area. An order of magnitude is 1μm². Contacting this very small active region to the external circuit has also to be made by means of low parasitic interconnecting techniques. In practice, this implies the use of air bridge contacting technology which is quite common in MMIC technology but requires real skill on micron and submicron scales. On the basis of such an integration, Figure 2 gives the current-voltage characteristic measured at 300 K for a 1μm² area InP-based RTD. The peak current density is higher than 200 kA/cm² for a peak-to-valley current ratio of typically 9:1. These are state -of -the art results.

### 3. HETEROSTRUCTURE BARRIER VARACTORS

Basically, It can be recognized that Heterostructure Barrier Varactors (HBV's) have potential advantages over their Schottky counterparts and very promising results have been reported in the literature <sup>3-5</sup>. The key advantage is the symmetry of the capacitance-voltage characteristic about zero-Volt. Such symmetry improves dramatically the functionality of devices since only odd harmonics are generated in harmonic multiplication. Symmetrical C-V relationship can also be achieved with back-to-back Schottky's but its was shown that self-biasing effects impede the variation of elastance when the devices are driven in a large signal regime. Secondly, several degrees of freedom are afforded by the use of semiconductor heterojunctions and novel structures, notably those making use of a quantum well/barrier or a delta doping configuration can be fabricated to tailor the C-V characteristics. Another important advantage stems from the fact that the devices can be vertically stacked during epitaxy. This epitaxial integration is a welcome feature in terms of voltage handling and capacitance levels.

In order to illustrate the design rules, let us consider the epitaxial material depicted in Figure 3 grown by gas source molecular beam epitaxy, starting from a semi-insulating Fe-doped InP substrate. Two basic In<sub>0.53</sub>Ga<sub>0.47</sub>As /In<sub>0.52</sub>Al<sub>0.48</sub>As /AlAs /In<sub>0.52</sub>Al<sub>0.48</sub>As /In<sub>0.53</sub>Ga<sub>0.47</sub>As layered structures were series integrated during the same epitaxy <sup>6-7</sup>. It can be shown that the device characteristics scale with epilayer complexity. Hence, the voltage breakdown is twice that of the single barrier device whereas the capacitance is half the value for one barrier. Figure 4 displays the nonlinarity achieved experimentally for two barriers in series which correspond to a Dual Heterostructure Barrier Varactor (DHBV). The symmetry in the C-V characteristic is excellent. This is advantageous for efficiently rejecting the even harmonics. The zero-bias voltage is 1fF/μm². The capacitance ratio is 6:1 Also plotted in Figure 4 is the voltage dependence of the conductance of the device. Note the unit of the conductance in nS/μm². The voltage handling of such a device is thus remarkable with a "safe" peak-to-peak operating voltage range of at least 20 V.

X 2

|               |                                    |       |
|---------------|------------------------------------|-------|
| InGaAs        | $5 \times 10^{14} \text{ cm}^{-3}$ | 500nm |
| InGaAs        | $1 \times 10^{17} \text{ cm}^{-3}$ | 300nm |
| InGaAs        | Undoped                            | 5nm   |
| InAlAs        | Undoped                            | 5nm   |
| AlAs          | Undoped                            | 3nm   |
| InAlAs        | Undoped                            | 5nm   |
| InGaAs        | Undoped                            | 5nm   |
| InGaAs        | $1 \times 10^{17} \text{ cm}^{-3}$ | 300nm |
| InGaAs        | $5 \times 10^{18} \text{ cm}^{-3}$ | 500nm |
| InP Substrate |                                    |       |

Figure 3 Growth sequence for HBV's in Dual barrier configuration

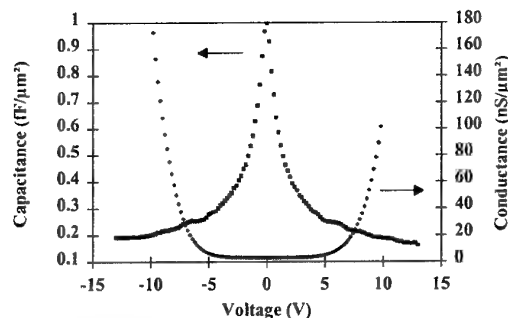


Figure 4 : Capacitance and conductance versus voltage for a dual barrier InP-based heterostructure. The capacitance ratio is 6:1 whereatg

The multiplier block used for the tripler measurements at 250 GHz is a crossed wave guide type mount with wave-guides coupled through a low-pass stripline filter. The pump power incident in the full-height WR-8 waveguide is fed to the planar integrated diode through a stripline E-plane transition and through the low pass filter implemented on a 75  $\mu\text{m}$ -thick quartz substrate. Impedance matching at input and output ports is achieved using two sliding non contacting backshorts. We used the devices whose Scanning Electron Micrograph (SEM) is displayed in Figure 5. The diodes were mounted in a flip-chip technology and tested at Ecole Normale Supérieure in France and at Rutherford Appleton Laboratory in United Kingdom. Figure 6 shows the variations of output power and conversion efficiency versus pump power measured at RAL Record performances have been obtained for these InP-based HBV's <sup>8</sup>.

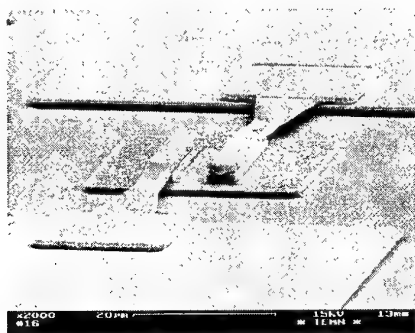


Figure 5 Scanning Electron Microphotograph for a quadruple barrier device.

RAL Frequency Tripler HBV-2 @ 246GHz Using a Lille 2x4x12μm INP HBV

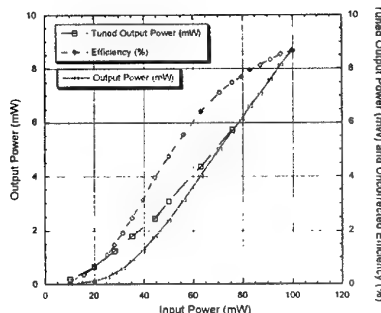


Figure 6: Conversion efficiency and output power versus input power measured @250 GHz.

In comparison to our previous experiment with  $2 \times 4 \times 12 \mu\text{m}^2$  samples reported previously <sup>5</sup> with 5% efficiency and 5mW output power at 216 GHz a significant increase in efficiency and frequency capability has been achieved. No saturation effects in the output power variation versus input power can be seen and it is believed that much higher power could be delivered at higher pump level.. At a last comment, let us mention that the second harmonic content was found to be -25 dB below the third harmonic. This very good rejection of the even harmonic is a direct consequence of the excellent symmetry in the capacitance-voltage characteristics. In the short term, it is believed that this very good performances with simultaneously high output power and efficiency can be further improved with the rf testing of eight barrier samples.

#### 4. SCHOTTKY DIODES

The third key component in ultra high frequency nonlinear electronics is the Schottky diode which is notably used in heterodyne reception at room temperature. In that case, we take advantage of the exponential variation of current versus voltage under bias condition for down converting the rf signal. Also, subharmonically pumped mixers have exhibited excellent performances over the past at millimetre wavelengths with conversion efficiency only slightly worse than comparable fundamental mixers and this operating mode is often chosen. Successful operation of subharmonically pumped mixers requires an antiparallel configuration for mounting the diodes with a very good circuit balance. Towards this goal the monolithic integration of devices is imperative.

In this context, let us consider the processing techniques on the basis of a planar integration of the devices. The first requirement is the necessity to shrink drastically the lateral dimension of the diodes to meet the requirement first of a low capacitance and secondly to decrease as far as possible the series resistance. It can be demonstrated that a huge improvement can be obtained by implementing T-finger-shaped Schottky contacts surrounded by ohmic contact in close proximity, followed by a deep etch for decreasing the parasitic capacitance<sup>9</sup>. Figure 7 shows a Scanning electron microphotograph of the mould which served for fabricating the T gate whereas Figure 8 shows the completed device which was fabricated at IEMN.

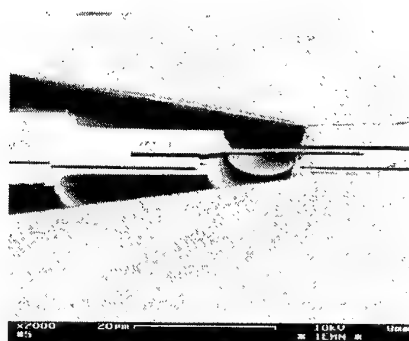
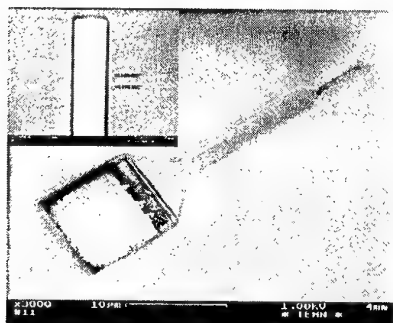


Figure 7 SEM of the mould which is used for processing in one step the contacting and interconnecting elements

Figure 8 SEM of a Schottky device planar integrated with T-shaped anode

These kind of devices relying on an InP technology have been successfully fabricated in several laboratories over the world and have shown promise for the down conversion under subharmonically condition at 200 and 500 GHz<sup>10-11</sup>.

## 5. CONCLUSION

In conclusion, the Terahertz field has now experience a profound change resulting from the recent advances in the growth of multi-layered heterostructure on short scales and in planar integration techniques. For each non linear functions involved in heterodyne reception and more generally in front end, some novel devices can be implemented which now compete in terms of frequency capability and/or power delivering with respect to more conventional devices. The use of semiconductor heterostructures appears vital in the improvement of performances and for the enhancement of functionality.

## 6. ACKNOWLEDGMENT

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## Resonant Tunneling Diodes for High-Speed Trigger Applications

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Resonant tunneling diodes (RTDs) are modelled for further circuit simulations and design like high-speed trigger-circuits and other switching applications. In addition to the current-voltage characteristics, our model considers also the actual capacitance of the device which was mostly considered constant or taken as the classical capacitance of the device similar to a pn-junction. The model can be used with different circuit simulators without any convergence difficulties. The simulated results have been compared with DC measurements and preliminary switching experiments on RTDs fabricated at the University of Ulm.

Due to differences between measured and estimated characteristics of RTDs, models based on measured results have been adopted. Several authors have used approximations for the current through an RTD, mainly based on mathematical approximation and measured results [1]. The current through an RTD is

$$I(V) = C_1 V^i \{ \tan^{-1}[C_2(V - V_1)] - \tan^{-1}[C_2(V - V_n)] \} + C_3 V^j + C_4 V^k.$$

The total capacitance of an RTD is

$$C_{tot}(V) = A_1(1 - V/V_1)^n + A_2 \exp(-(\frac{V-V_2}{A_3})^2)$$

The constants in both equations are determined using the measured current and capacitance of the device.

RTDs used throughout this work were grown with MBE on SI InP substrates, spacer layers were used to prevent doping of the QW and the barriers and to decrease the total capacitance of the device by increasing the depletion region length. Diode mesas were defined by optical lithography and wet chemical etching, then Ni/Ge/Au was deposited to form the two ohmic contacts to the device. Planar pads are connected to the diode contacts via air-bridges for the central pad.

Fig.1 shows measured current and capacitance of an RTD. The peak in the negative differential resistance (NDR) range is a consequence of the charge buildup in the QW. In some applications, a large capacitance increases the switching time of the device which degrades the performance of the device. In other applications, the peak in the capacitance can be desirable where a large change in the reactive component of the diode takes place as in frequency multipliers; this change can be useful in increasing the efficiency.

<sup>1</sup>Department of Semiconductor Physics

Results of the measurements are added to the simulators ELDO (a SPICE-like time-domain simulator) and MDS for the purpose of transient analysis of trigger circuits for sampling oscilloscopes. Fig.2 shows the simulated results whereas Fig.3 shows the measured results of the realized circuit (shown in Fig.4); both simulated and measured results show large similarity.

RTD model with capacitance consideration is used to understand different RTD applications and judge their transient analysis which serves also as a feedback to design RTDs with other parameters.

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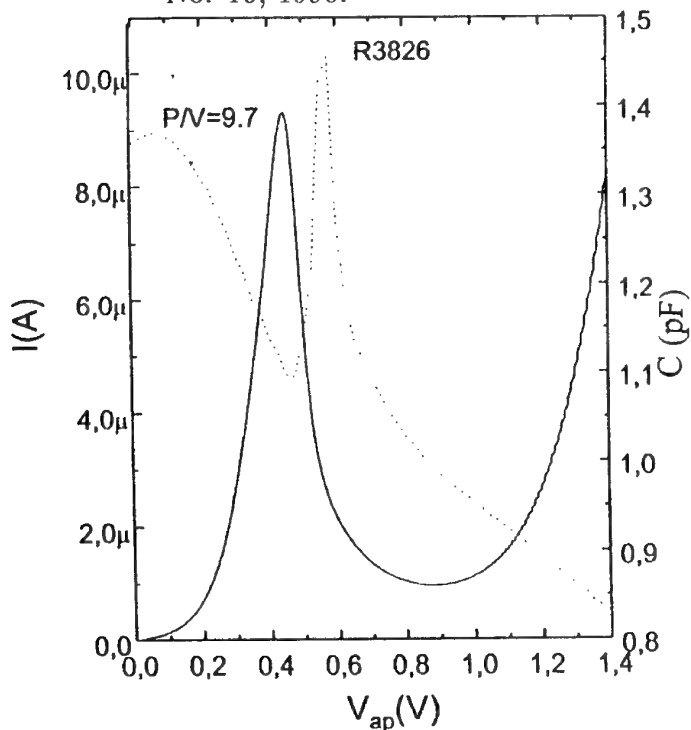


Fig.1: Measured current and capacitance of an RTD

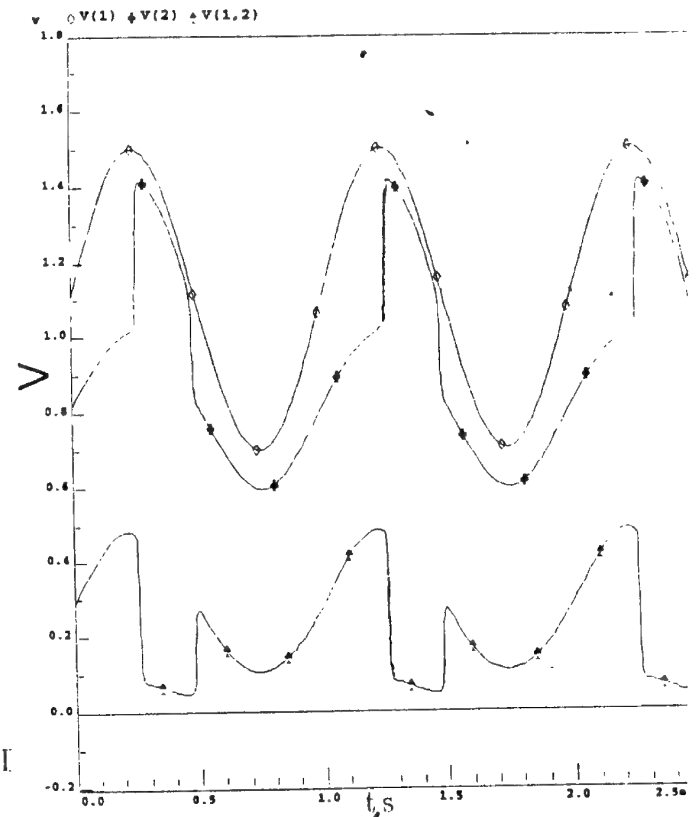


Fig.2: Simulated circuit signals using RTD-mod

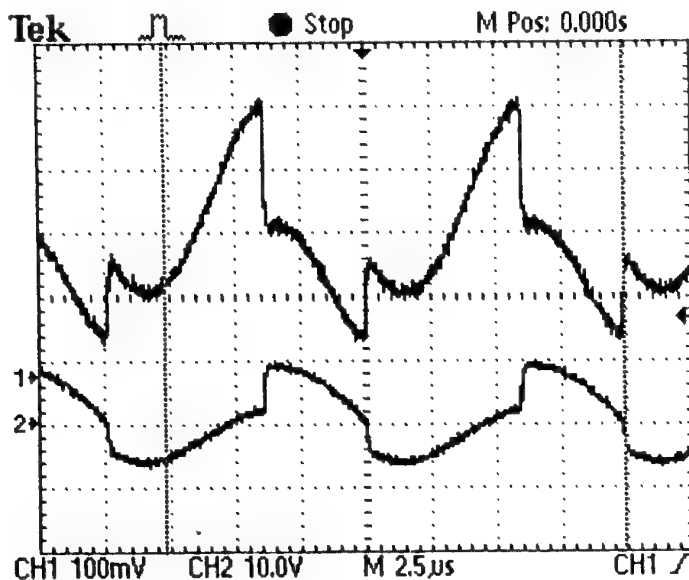


Fig.3: Measured circuit signals

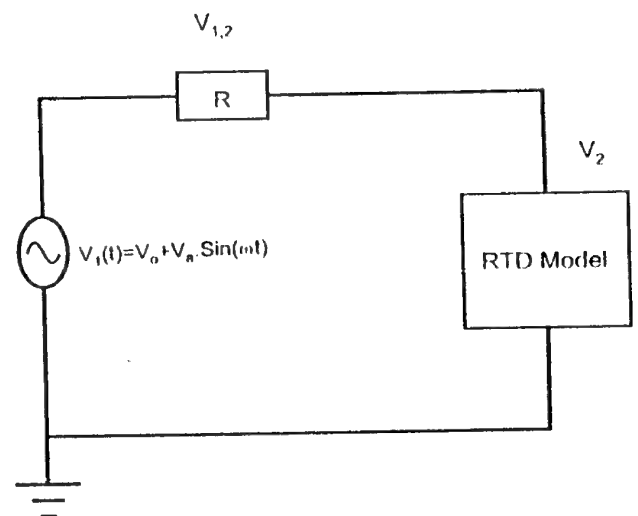


Fig.4: Circuit used in simulations and measurements

# A 150 GHz MMIC Receiver Array with On-Chip Pumping-Power Distribution for Plasma ECE Diagnostics

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## I.- Introduction.

Spatially resolved measurements of electron-temperature fluctuations in hydrogen plasmas are a key in the investigation of both heat transport and the turbulent confinement [1]. The development of detector arrays for 2D ECE imaging [2] represents today therefore one of the main concerns of plasma diagnostics.

The design of a fully MMIC 150 GHz subharmonic mixer array to be installed in the W7-AS at Garching (Germany) is here presented. The circuit is realised on a multi-substrate technology and includes aperture-coupled patch antennas for the reception of the plasma signal.

As opposed to other similar-purpose arrays realised to date (e.g. [3]), which make use of quasi-optical techniques, the circuit distributes local oscillator power on the chip, thereby reducing significantly pumping-power level requirements. Cross-talking between channels is improved by physical substrate separation to prevent propagation of substrate modes. Also patch antennas can be isolated to increase channel isolation. Finally, the circuit should present a 9 GHz bandwidth at RF and IF, allowing for simultaneous temperature profiles at different values of plasma radius [4].

## II.- System Concept.

The MMIC circuit is made of four parallel subharmonic Schottky-diode mixers realised on microstrip line on a 70- $\mu\text{m}$  thick GaAs substrate as shown in figure 1. Each channel receives plasma radiation in the band 144 to 153 GHz through a patch antenna coupled to the microstrip circuit by means of a slot on the ground plane. The antenna is printed on a 150- $\mu\text{m}$  thick fused quartz substrate using a thin-film technology. The total size of the chip is about 10 x 6 mm<sup>2</sup>.

Local-oscillator (at 67.5 GHz) power is coupled to a 50  $\Omega$  microstrip line on the chip and distributed uniformly between channels using a two-stage power splitter. Each stage of the divider was analysed using a commercial software implementation of the method of moments [5], then the two-stage structure was also

checked. LO distribution loss include 2 dB conductor & dielectric loss (3 dB/cm @ 67.5 GHz) and 2 dB from the LO filter. The advantage of on-chip distribution in the case of the linear array may be best understood by comparing this value with LO loss inherent to quasi-optical transmission. In the system described, assuming an antenna equivalent surface of 4 x 0.16 mm<sup>2</sup> spread along a 5 mm length, LO loss would reach up to a minimum of 15 dB unless non-cylindrical optical systems are implemented.

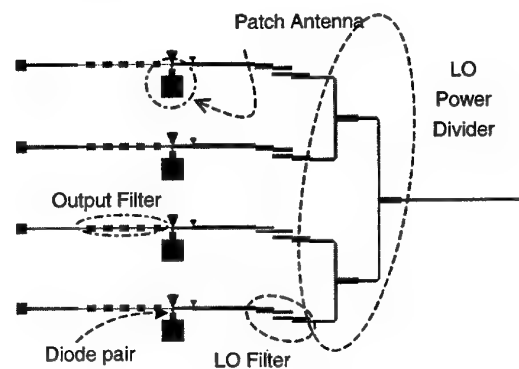


figure 1: Circuit layout

An anti-parallel structure has been chosen for the diode configuration. This topology has well-known advantages ([6],[7]) and is still being employed for different applications and at different frequency ranges ([8], [9]). The reduction of the pumping frequency lowers in our case the power restrictions, since sources at about 70 GHz are more readily available than in the 150 GHz region. Furthermore, filtering of the image band is simplified as the need to match an LO signal lying between RF and image bands is eliminated.

A typical problem of subharmonic mixers is unnecessary conversion loss due to possible diode asymmetries. The proposed MMIC technology allows to overcome this disadvantage since diodes are identically and simultaneously processed.

## III.-Mixer Diodes

The anti-parallel diode pairs used as mixer elements are an evolution of those described in [9]. The air bridge is

substituted by an anode finger which runs above a 1.5 to 2- $\mu\text{m}$  thick passivation layer. This protects the diode further from physical damage. The ohmic contact, in turn, is realised from the front side in order to simplify the technological process. Contact pads are not necessary since the diodes are integrated on the microstrip line, eliminating an important contribution to parasitic capacitance.

#### IV.- Mixer Design

The goal of the design is to obtain the smallest conversion loss, with rejection of unwanted harmonics (fundamental mixing, image) and good isolation between ports.

Performance of the mixer, specially in terms of conversion loss, is fixed by the design of the filtering and matching networks on each side of the diode pair [10]. The LO signal is injected through a microstrip structure which operates as LO filter and presents to the diodes a short circuit at IF and RF. Another structure on the other side acts as IF filter and LO short. The RF antenna is also coupled to this structure.

The Schottky diodes employed have been introduced in the simulator with an equivalent circuit which contains a linear part, estimated from measurements and physical dimensions, and a non-linear part, based on measurements.

The microstrip parts have been simulated with the standard equivalent circuit models, but also with an electromagnetic simulator using the method of moments to take into account additional coupling effects. This is crucial to prevent unwanted changes of the desired characteristics, more important at higher frequencies.

#### V.- Simulated Performance

Conversion loss was evaluated in a single channel using harmonic balance techniques [11], in the whole RF band for several LO power values. The ripple across the RF band is less than 4 dB for each case. Conversion loss saturate beyond 5 dBm pumping power per diode pair. For LO available power ranging from 5 dBm to 10 dBm, best simulated values of conversion loss vary between 8 dB and 6 dB. This can be considered as an optimistic estimation. Single diodes were included to be characterised on wafer, making possible a more accurate post-simulation.

Conversion loss versus IF frequency for several LO power values are shown in figure 2. Typical values of isolation between ports were also estimated. The LO-IF isolation is 31 dB. The LO power flowing towards the RF antenna is 41 dB below the injected LO level. The RF-IF isolation is 50 dB.

Undesired down-converted image signal at the IF port is between 10 and 30 dB below the desired IF frequency. This is due to the antenna acting as an image filter and to additional intended mismatching. The third-order interception point occurs for -6 dBm

of output power (8 dBm LO power, RF at 149 GHz). This means that for an optimistic value of -30 dBm of RF input power the third-order harmonic products at the output are more than 70 dB below the IF signal.

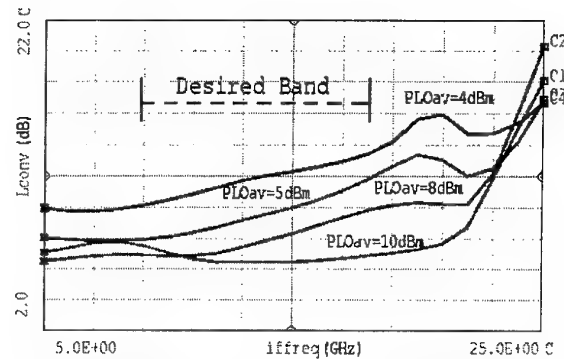


figure 2: Simulated conversion loss versus output frequency for different values of pumping power available per channel.

#### VI.- Conclusions

A new approach to LO-power supply in multi-channel imaging arrays at millimeter-wave frequencies is proposed. Use of subharmonic pumping combined with on-chip power distribution may reduce power requirements by a factor of more than 10 dB and simplifies image-band filtering.

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# „Hot Electron Injection Field Effect Transistor“

by

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## Abstract

The purpose of the work reported is to experimentally prove the idea that the upper frequency limit of a field effect transistor can be significantly increased by replacing the highly doped source contact by a hot electron injection contact of the type used in the planar injection limited Gunn diode, the so-called „field effect controlled transferred electron device“ or „FECTED“[1]. The injection limiting contact which consists of an ohmic contact and an overlapping Schottky gate injects hot and, hence, fast electrons into the FET-channel thereby drastically reducing the total transit time through the channel. The new FET, which is called „hot electron injection field effect transistor“ or „HEIFET“\* is not subject to the slow acceleration process electrons experience when injected from a highly doped source contact (the standard source contact of conventional field effect transistors) where the electric field and, hence, the velocity of electrons is low. The time to accelerate slow electrons in GaAs MESFETs can be as large as a few picoseconds due to the slow energy transfer (energy relaxation) time. This is in our opinion the reason why 0,5 $\mu$ m gate-MESFETs exhibit a low  $f_T$  ( $\approx 15$ GHz) although the time electrons need to travers a distance of 0,5 $\mu$ m at saturated velocity ( $\approx 10^7$ cm/s) is only 5ps which is one third of the RF cycle at 60GHz and which should be short enough to allow efficient operation of a 0,5 $\mu$ m gate-MESFET at 60GHz.

Experimental results obtained with 0,5 $\mu$ m gate-HEIFETs at 60GHz will be presented and compared with the theoretical predictions.

## Acknowledgements

This work is supported by the Austrian Science Foundation (FWF) under contract No. P12702 TEC and the Austrian Microelectronics Society (GMe).

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„A 60GHz MMIC-compatible TED-Oscillator“,  
IEEE Microwave and Guided Wave Letters, vol. 5, no. 4, April 1995, pp. 114–116,

## MODULATION RESPONSE PREDICTIONS FOR A DUAL CHANNEL SiGe FET

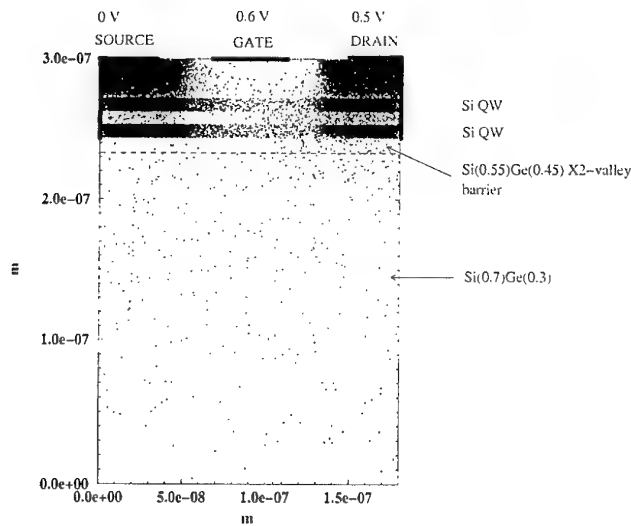
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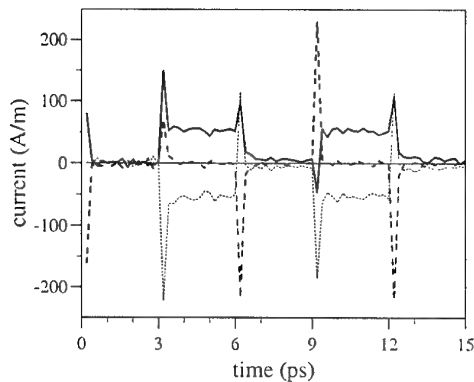
Monte Carlo simulations have been used to model strained Si/SiGe field effect transistors with submicron Schottky gates, with the intention of designing a picosecond/terahertz device. The devices that will be reported are of the kind shown in figure 1. In this example, there are two 90Å thick layers of tensile strained Si sandwiched between  $\text{Si}_{0.7}\text{Ge}_{0.3}$ , which form two X2-valley quantum wells for electrons. A 90Å thick layer of compressive strained  $\text{Si}_{0.55}\text{Ge}_{0.45}$  is grown alongside the lower Si well, with the aim of reducing the dispersion of more energetic ( $> 0.2$  eV) X2-valley electrons into the SiGe substrate. The main purpose behind the heterostructure is to confine most of the charge flowing under the gate to the X2-valleys. In addition to the X2-X4 valley strain splitting ( $\sim 0.2$  eV) and the comparatively light effective mass associated with Si X2-valley quantum well subbands ( $0.196m_0$ ), other properties which are intended to produce a rapid modulation response are the short  $0.08\text{ }\mu\text{m}$  conduction channel under a  $0.05\text{ }\mu\text{m}$  gate and the pronounced velocity overshoot in strained Si compared to unstrained Si. Apart from the layer structure, this compact device is comparatively simple, without modulation doping effects alongside the Si channels.

Square wave switching of the gate voltage suggests that an operating device of the kind in figure 1 should have a high intrinsic speed. Steady 'high' or 'low' drain current states are reached within 1 ps of reversing the gate bias - as indicated by the rapid decay of the electric displacement which forms the gate current in figure 2. Operating with drain-source biases  $\sim 0.5$  V, there is not significant scattering of electrons in Si into the X4-valleys ( $\sim 20\%$  fractional occupation in the gate-drain region of the channels), and the X2-valley barrier of the  $\text{Si}_{0.55}\text{Ge}_{0.45}$  layer assists in channelling heated carriers towards the drain instead of the substrate.

Simulations of the effect of modulating the gate bias will be reported to demonstrate the device's transient response and gain bandwidth. For this analysis, a sinc voltage pulse is applied, which has a flat frequency spectrum up to the frequency defined by the oscillation period during the pulse. The choice of ten cycles over a simulated 10 ps period provides a frequency analysis up to 1 THz with 100 GHz resolution. The current gain is obtained by dividing the elements of the Fourier transforms of the drain and gate current signals recorded over the complete sinc pulse.



**Figure 1:** Device geometry of the proposed Si/SiGe dual channel FET, showing the instantaneous distribution of 30000 electron particles used in the simulations. The doping under the source and drain is  $2 \times 10^{24} \text{ m}^{-3}$ .



**Figure 2:** Demonstration of current switching at 300 K for the device of figure 1. The device is switched off (unbiased) during the interval  $t = 0 - 3 \text{ ps}$ . From  $t = 3 \text{ ps}$ , a steady drain-source bias of 0.5 V is applied, but at 3 ps intervals, the gate voltage is switched between +0.4 and -0.4 V. The solid bold curve represents the drain current, the dashed bold curve transient electric displacement current at the gate, and the faint dashed curve the current response at the source contact. Note that the device switches completely between the 'high' and 'low' current states within 1 ps. Rapid switching is aided by transient overshoot behaviour in the Si channels.

## Piezoelectric and Optical Properties of Strained InGaAs/GaAs Quantum Well Structures Grown by MOVPE on (111)A GaAs Substrates

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The growth of compound semiconductor structures in the non-conventional  $\langle 111 \rangle$  crystallographic directions has received increased attention due to their special properties and potential for novel optoelectronic devices. We have recently reported [1] the first successful fabrication of high quality GaAs/AlGaAs Multiple Quantum Well (MQW) structures on (111)A GaAs substrates by the Metalorganic Vapor Phase Epitaxy (MOVPE) process. In this work, we report the structural and optical properties of strained InGaAs/GaAs Quantum Wells (QW) grown by MOVPE on (111)A GaAs substrates. A distinctive property of  $\langle 111 \rangle$  strained QWs is the presence of a strong piezoelectric field in the wells with a concomitant effect on the barrier field.

Strained InGaAs/GaAs QW structures with nominal well widths of 40 Å were grown by atmospheric pressure MOVPE on (111)A GaAs. A High Resolution X-Ray Diffractometry (HRXRD) study was carried out to accurately determine the QW structural parameters. Room temperature Photoreflectance (PR) spectroscopy, which permits the observation of higher interband transitions, was used to assess the abruptness and uniformity of the QW heterointerfaces. The PR spectra show all the possible interband transitions and, also, Franz-Keldysh oscillations, which were analyzed to obtain the electric field in the barriers. A theoretical computation appropriate for  $\langle 111 \rangle$  oriented structures, incorporating the piezoelectric field in the wells, as well as the modified barrier field, was used to obtain all the confined electron and hole energies and, thereby, interpret the PR analysis. The theoretically calculated transition energies are in very close agreement with those experimentally obtained by fitting the PR spectra even up to the highest possible transitions for these wells. From a detailed well width Monolayer (ML) analysis, it is demonstrated that the QW interfaces have  $\pm 1$  ML roughness and that the interfaces are very abrupt and uniform. Photoluminescence (PL) measurements were also used to further assess the optical quality and interface quality by determining the Full-Width-at-Half-Maximum (FWHM) values. A PL FWHM of 9.1 meV was observed, which corresponds to at most a  $\pm 1$  ML fluctuation in well width. To our knowledge, this is the first demonstration of very high quality MOVPE grown InGaAs/GaAs QW structures on (111)A GaAs substrates.

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# Author index

| <b>A</b>          |              | <b>C</b>       |            |
|-------------------|--------------|----------------|------------|
| R.A. Abram        | 147          | F. Calle       | 133        |
| M. Achouche       | 101          | T. Camps       | 103        |
| R. Adde           | 49           | C. Canali      | 47         |
| E. Alekseev       | 121, 129     | A. Cappy       | 75         |
| Y.H. Aliyu        | 65           | D. Cassagne    | 91         |
| I.M. Al-Ofi       | 65           | N. Cavassilas  | 49         |
| P. André          | 109          | A. Cazarre     | 103        |
| F. Aniel          | 49           | J-L. Cazaux    | 77         |
| V. Aninkevicius   | 55           | S. Cho         | 149        |
| G. Apercé         | 75           | P.P. Chow      | 123        |
| G. Archontopoulos | 95           | B. Cogo        | 77         |
| A. Arendarenko    | 67           | P. Cova        | 47         |
|                   |              | Y. Crosnier    | 61, 127    |
|                   |              | G.C. Crow      | 147        |
| <b>B</b>          |              | <b>D</b>       |            |
| W. Bächtold       | 97           | Y. Danto       | 45         |
| J.P. Bailbé       | 103          | I. Daumiller   | 131        |
| M. Beck           | 27           | J.P.R. David   | 33         |
| J-L. Benchimol    | 109, 111     | T. Decaesteke  | 75         |
| H. Benisty        | 87           | J. Décobert    | 49, 51, 81 |
| P. Berdager       | 109, 111     | R.M. De La Rue | 87         |
| C. Bergamaschi    | 107          | C. Delseny     | 53         |
| M. Bergmair       | 145          | D. Demange     | 79         |
| T. Bergunde       | 101          | S. Demichel    | 113        |
| S. Biblemont      | 81           | D. Dieci       | 47         |
| K. Bitzer         | 141          | R. Dietrich    | 123        |
| S. Blayac         | 53, 109, 111 | C. Diskus      | 145        |
| S. Bollaert       | 75           | A-M. Duchenois | 109, 111   |
| B. Bonte          | 61           | JM. Dumas      | 45         |
| S. Boret          | 75           | W. Dürr        | 17         |
| P. Boucaud        | 49           |                |            |
| B. Boudart        | 61, 127      | <b>E</b>       |            |
| D.P. Bour         | 27           | L.F. Eastman   | 125        |
| G. Brémond        | 51           | P. Ebele       | 17         |
| T.A. Briantseva   | 63           | A. Eisenbach   | 121        |
| F. Brunner        | 101          | U. Erben       | 17         |
| D. Buttari        | 39           |                |            |

**F**

|                   |     |
|-------------------|-----|
| J. Faist          | 27  |
| A. Förster        | 93  |
| A. Fox            | 93  |
| M. François       | 81  |
| M.L. de la Fuente | 143 |

**G**

|                |          |
|----------------|----------|
| C. Gaquière    | 127      |
| B. Georgescu   | 51       |
| P. Gibart      | 133      |
| K.D. Glinchuk  | 83       |
| J. Godin       | 109, 111 |
| Z.S. Gribnikov | 31       |
| D.E. Grider    | 129      |
| B. Grimbert    | 75       |
| G. Guillot     | 51       |

**H**

|                |     |
|----------------|-----|
| S. Hahle       | 101 |
| H.L. Hartnagel | 143 |
| U. Hodel       | 93  |
| V. Hoel        | 75  |
| D. Hofstetter  | 27  |
| O. Homan       | 97  |
| R.C.P. Hoskens | 95  |
| R. Houdré      | 87  |
| J.M. van Hove  | 123 |
| X. Hue         | 61  |
| A. Huber       | 107 |
| D. Huber       | 107 |
| F. Huet        | 127 |

**I**

|          |    |
|----------|----|
| Y. Ishii | 21 |
|----------|----|

**J**

|             |     |
|-------------|-----|
| H. Jäckel   | 107 |
| H. Jacobs   | 97  |
| S.G. Jarrix | 53  |
| W. John     | 101 |
| C. Jouanin  | 91  |

**K**

|              |          |
|--------------|----------|
| N. Käß       | 123      |
| T. Kazior    | 71       |
| B.W. Kim     | 149      |
| J. Kim       | 149      |
| E. Kohn      | 123, 131 |
| M.F. Kokorev | 59       |
| E. Kolmhofer | 145      |

|                |     |
|----------------|-----|
| P. Kordos      | 93  |
| A.N. Korshak   | 31  |
| S. Kraus       | 101 |
| T.F. Krauss    | 87  |
| M. Kunze       | 141 |
| P. Kurpas      | 101 |
| A.G. Kuzmenkov | 59  |

**L**

|                  |     |
|------------------|-----|
| N. Labat         | 45  |
| D. Labilloy      | 87  |
| C. Ladner        | 81  |
| C. Lanzieri      | 47  |
| A. Laugier       | 35  |
| R. Leblanc       | 79  |
| J.L. Leclercq    | 91  |
| H. Leier         | 123 |
| S. Lepilliet     | 75  |
| X. Letartre      | 91  |
| K.F. Li          | 33  |
| J. Liberis       | 55  |
| C.I. Lin         | 143 |
| D.V. Lioubchenko | 63  |
| D. Lippens       | 137 |
| N.M. Litovchenko | 83  |
| B. Ljevar        | 95  |
| P. Llinares      | 53  |
| F. Lopez         | 143 |
| K. Luebke        | 145 |
| V.E. Lyubchenko  | 63  |

**M**

|               |        |
|---------------|--------|
| H. Maher      | 49     |
| M. Mai        | 101    |
| A. Majerfeld  | 149    |
| N.A. Maleev   | 59     |
| J. Malin      | 77     |
| C. Maneux     | 45     |
| M. Maretto    | 39     |
| M. Marso      | 93     |
| A. Marty      | 103    |
| G. Massari    | 39     |
| A. Matulionis | 55     |
| J-P. Medus    | 111    |
| G. Meneghesso | 39, 47 |
| R. Menozzi    | 47     |
| V.V. Mitin    | 31     |
| F. Mollot     | 105    |
| E. Monroy     | 133    |
| T. Morf       | 107    |
| D.V. Morgan   | 65     |

|           |     |
|-----------|-----|
| M. Muller | 81  |
| E. Muñoz  | 133 |

## **N**

|               |     |
|---------------|-----|
| H.C. Neitzert | 43  |
| C. Nguyen     | 129 |
| N.X. Nguyen   | 129 |
| L.T. Nuyen    | 15  |

## **O**

|             |        |
|-------------|--------|
| U. Oesterle | 27, 87 |
| F. Omnès    | 133    |
| D.S. Ong    | 33     |

## **P**

|                    |          |
|--------------------|----------|
| F. Pardo           | 105, 113 |
| F. Pascal          | 53       |
| J.P. Pascual       | 143      |
| D. Pavlidis        | 121, 129 |
| J-L. Pelouard      | 105, 113 |
| A. Penarier        | 53       |
| A. Piccirillo      | 43       |
| M.A. Poisson       | 127      |
| G. Post            | 51, 81   |
| P. Pottier         | 91       |
| A.V. Prokhorovitch | 83       |
| M. Py              | 51       |

## **R**

|                      |              |
|----------------------|--------------|
| G.J. Rees            | 33           |
| M. Remram            | 35           |
| D. Rentner           | 101          |
| E. Richter           | 101          |
| M. Riet              | 45, 109, 111 |
| F. Robin             | 97           |
| P.N. Robson          | 33           |
| M. Rodríguez-Gironés | 143          |
| T.G. van der Roer    | 95           |
| M. Rohner            | 107          |
| D. Roques            | 77           |

## **S**

|                 |         |
|-----------------|---------|
| S. Sainson      | 81      |
| A. Sanz-Hervás  | 149     |
| J-C. Sarkissian | 77      |
| N. Saysset      | 45      |
| A. Scavennec    | 45, 49  |
| K-B Schad       | 17      |
| P. Schmid       | 131     |
| H. Schumacher   | 17, 141 |
| V. Schwarz      | 107     |
| C. Seassal      | 91      |

|                |     |
|----------------|-----|
| L. Semra       | 35  |
| D. Shaw        | 77  |
| D. Sicault     | 105 |
| A. Simon       | 143 |
| D. Simpson     | 77  |
| C.J.M. Smith   | 87  |
| E. Sönmez      | 17  |
| A. Souifi      | 51  |
| M. Soulard     | 77  |
| P. Souverain   | 103 |
| T. Spitzbart   | 101 |
| A. Stelzer     | 145 |
| A. Stemmer     | 97  |
| O.N. Strilchuk | 83  |
| E. Strobel     | 131 |
| Y. Sveshinikov | 67  |

## **T**

|                 |          |
|-----------------|----------|
| J. Tasselli     | 103      |
| R. Teissier     | 105, 113 |
| D. Théron       | 127      |
| H. Thim         | 145      |
| V.I. Tolstikhin | 95       |
| A. Touboul      | 45       |
| R.C. Tozer      | 33       |
| G. Tränke       | 101      |
| S. Trassaert    | 127      |
| P. Tronc        | 149      |

## **V**

|                 |     |
|-----------------|-----|
| A. Vescan       | 123 |
| C. Villar       | 149 |
| P. Viktorovitch | 91  |

## **W**

|              |     |
|--------------|-----|
| X. Wallart   | 75  |
| N.G. Weimann | 125 |
| C. Weisbuch  | 87  |
| M. Weyers    | 101 |
| A. Wieszt    | 123 |
| H. Wittrich  | 101 |
| P. Wolter    | 101 |
| A.M. Wowchak | 123 |
| J. Würfl     | 101 |

## **Y**

|           |     |
|-----------|-----|
| F. Yousif | 141 |
|-----------|-----|

## **Z**

|             |     |
|-------------|-----|
| E. Zanoni   | 39  |
| J.C. Zolper | 117 |